# 内置BOOST升压的11W I²S输入D类音频功放

## 11W I²S Input, Mono Class D Amplifier with Boost Converter

## ■ FEATURES

- Power supply:
  - Power input $V_{BAT}$: 2.5V – 5.5V;
  - Adjustable Boost Voltage PVDD: up to 7.5V
  - DVDD/AVDD: 3.3V
- Audio Performance
  - 9.0W (VBAT=3.7V, PVDD = 7.5V, RL=3Ω, THD+N=10%)
  - 11.0W (VBAT=3.7V, PVDD = 7.5V, RL=2Ω, THD+N=10%
  - 5.5W (VBAT=3.7V, PVDD = 6.5V, RL=4Ω, THD+N=10%)
- Flexible Audio I/O
  - I²S, LJ, RJ, TDM input
  - 8, 16, 32, 44.1, 48, 88.2, 96, 192kHz Sample Rates
- General Operational Features
  - Hardware or Software Control mode
  - 4 Programmable I²C Addresses
- Robustness Features
  - Clock Error, Over Voltage, Over Current, and Overtemperature Protection
- Packages: Pb-free Packages, QFN28L-5×5

- 电源供电
  - 升压输入$V_{BAT}$: 2.5V – 5.5V;
  - 升压输出PVDD可调，最高7.5V
  - DVDD/AVDD: 3.3V
- 音频性能
  - 9.0W (VBAT=3.7V, PVDD = 7.5V, RL=3Ω, THD+N=10%)
  - 11.0W (VBAT=3.7V, PVDD = 7.5V, RL=2Ω, THD+N=10%
  - 5.5W (VBAT=3.7V, PVDD = 6.5V, RL=4Ω, THD+N=10%)
- 灵活的音频输入：
  - I²S, LJ, RJ, TDM 输入
  - 8, 16, 32, 44.1, 48, 88.2, 96, 192kHz 采样频率
- 其他功能
  - 硬件模式或软件控制模式
  - 4个I²C器件地址可选
- 保护：时钟错误、过压、过流、过温保护等
- QFN28L-5×5封装

## ■ APPLICATIONS

- Bluetooth/Wi-Fi Speakers
- Portable Speakers
- Smart speakers
- Smart Home
- 蓝牙/ Wi-Fi音箱
- 便携式音箱
- 智能音箱
- 智能家居

## ■ ORDERING INFORMATION

| Part Number | Package Type | Marking | Operating Temperature Range | MOQ/Shipping Package |
|---|---|---|---|---|
| HT5169SQER | QFN28L-5×5 | HT5169SQ<br>UVWXYZ[1] | -25℃～85℃ | Tape and Reel / 2500pcs |

[1] UVWXYZ is production tracking code

## ■ DESCRIPTION

The HT5169 is a mono Class D audio amplifier with multiple audio format port (I²S, LJ, RJ, TDM). It supports a variety of audio clock configurations (sample rate 8k – 192kHz).

HT5169 integrates a boost converter with a filter-less stereo class D audio power amplifier to provide 11W continuous power into a 2Ω speaker when operating from a Li-battery voltage boosted to 7.5V. Meanwhile, the boost output voltage is adjustable.

The HT5169 also includes hardware and software control modes and integrated digital clipper enable use in a multitude of applications.

Additionally, a thermally enhanced 28-Pin QFN provides excellent operation in the elevated ambient temperatures found in modern consumer electronic devices.

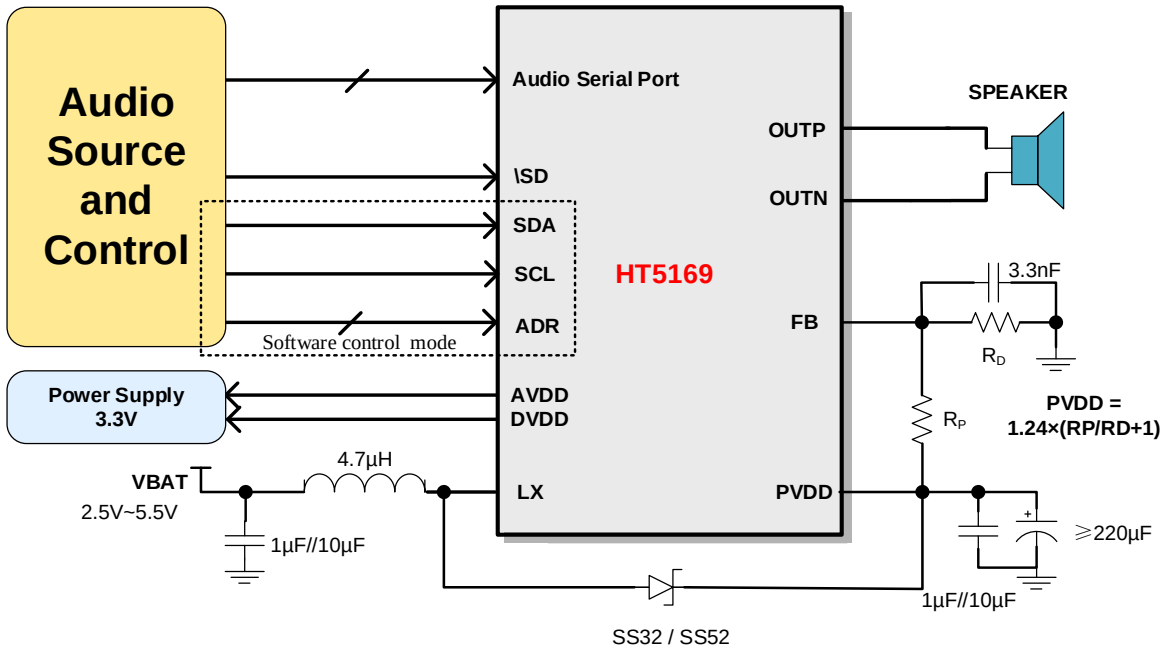
HT5169是一颗立体声D类音频功放，支持多种采样频率（8k-192kHz）、多种数字输入格式（I²S, LJ, RJ, TDM）。

HT5169是一款内置BOOST升压模块的D类音频功率放大器。内置的BOOST升压模块可通过外置电阻调节升压值，即使是锂电池供电，在升压至7.5V，2Ω负载条件下则能连续输出11W功率。其支持外部设置调节BOOST输出电压。

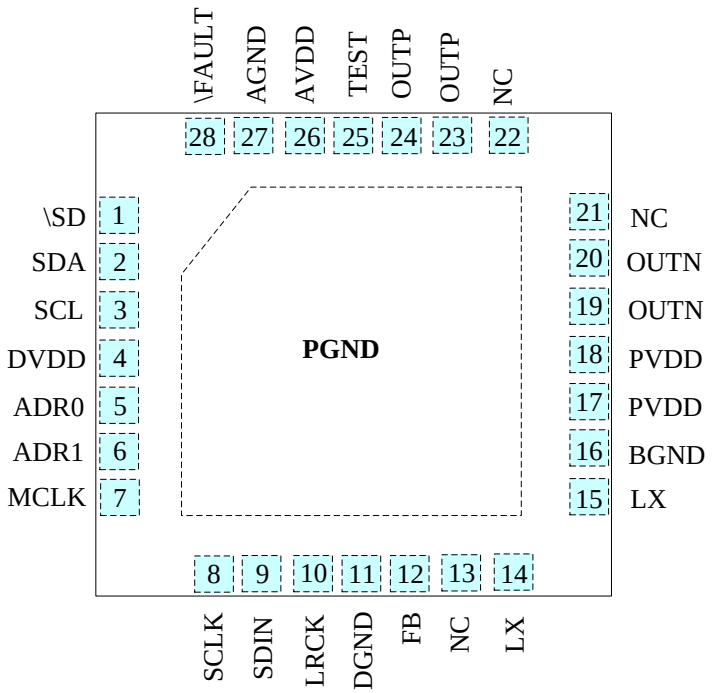
HT5169包含了硬件工作模式和软件控制模式，具有数字限幅器，支持不同应用。

该产品提供QFN28L-5×5封装，其具有不错的散热表现，在现代消费电子复杂的环境温度下提供出色的性能。

## ■ TYPICAL APPLICATION



## ■ TERMINAL CONFIGURATION




## ■ TERMINAL FUNCTION

| Terminal No. | Name | I/O[1] | Description |
|---|---|---|---|
| 1 | \SD | I | Places the speaker amplifier in shutdown mode while pulled low level. 接地时功放关闭 |
| 2 | SDA | I | I²C data input pin. I²C数据 |
| 3 | SCL | I | I²C clock input terminal. I²C时钟 |
| 4 | DVDD | P | Power supply for the internal digital circuitry. 数字电源端 |
| 5 | ADR0 | I | Determine the I²C Address of the device. I²C器件地址选择 |
| 6 | ADR1 | I | Determine the I²C Address of the device. I²C器件地址选择 |
| 7 | MCLK | I | Master Clock used for internal clock tree, sub-circuit/state machine, and Serial Audio Port clocking. 主时钟 |
| 8 | SCLK | I | Bit clock for the digital signal that is active on the serial data port's input data line. 串行时钟 |
| 9 | SDIN | I | Data line to the serial data port. 串行数据 |
| 10 | LRCK | I | Word select clock for the digital signal that is active on the serial port's input data line. 帧时钟，字段（声道）选择 |
| 11 | DGND | G | Ground for digital circuitry (NOTE: This pin should be connected to the system ground). 数字地 |
| 12 | FB | I | Regulator Feedback Input. 升压反馈点 |
| 13, 21, 22 | NC | / | No connection, connect GND for better thermal performance. 无电气连接，可接地 |

1 : I: Input; O: Output; G: Ground; P: Power; BST: BOOT Strap; OD: Open drain

| | | | |
|---|---|---|---|
| 14, 15 | LX | I | Internal Switch Input. 升压整流管输入 |
| 16 | BGND | G | Ground for boost converter circuitry (NOTE: This pin should be connected to the system ground). 升压电路地 |
| 17, 18 | PVDD | P | Boost Converter Output Voltage and Power Supply. 升压输出和功率电源 |
| 19, 20 | OUTN | O | Negative pin for differential speaker amplifier output. 输出负端 |
| 23, 24 | OUTP | O | Positive pin for differential speaker amplifier output. 输出正端 |
| 25 | TEST | O | Test pin leave it floating. 测试引脚，悬空。 |
| 26 | AVDD | P | Power supply for internal analog circuitry. 模拟电源端 |
| 27 | AGND | G | Ground for analog circuitry (NOTE: This pin should be connected to the system ground). 模拟地 |
| 28 | \FAULT | OD | Speaker amplifier fault terminal, which is pulled LOW when an internal fault occurs, open-drain output. 错误状态位，芯片发生某些错误时，该引脚拉低 |
| EP | PGND | G | Provides both electrical and thermal connection from the device to the board. A matching ground pad must be provided on the PCB and the device connected to it via solder. For proper electrical operation, this ground pad must be connected to the system ground. 既是地，又是散热PAD |

## ■ SPECIFICATIONS[1]

### ● Absolute Maximum Ratings [2]

| PARAMETER | Symbol | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Power supply voltage for AVDD | AVDD | -0.3 | | 4 | V |
| BOOST converter output voltage and Power supply voltage range | PVDD | -0.3 | | 7.8 | V |
| Power supply voltage for DVDD | DVDD | -0.3 | | 4 | V |
| DVDD Referenced Digital Input Voltages | $V_I$ | -0.3 | | DVDD+0.3 | V |
| Input terminal voltage range (IN+, IN-) | $V_{IN}$ | −0.6 | | PVDD+0.6 | V |
| Moisture Sensitivity Level (MSL) | | | MSL3 | | |
| Ambient Operating Temperature | $T_A$ | -25 | | 85 | ℃ |
| Junction Temperature | $T_J$ | -40 | | 125 | ℃ |
| Storage Temperature | $T_{STG}$ | -40 | | 125 | ℃ |

### ● Recommended Operating Conditions

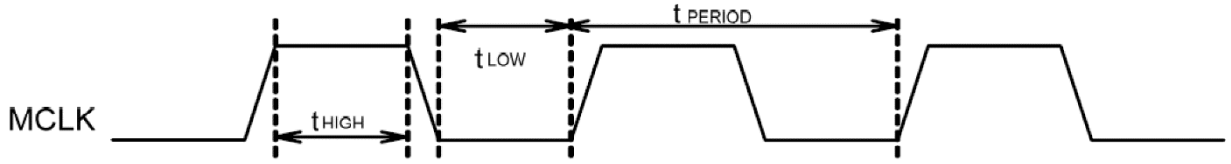
| PARAMETER | Symbol | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Power supply voltage for AVDD | AVDD | | 3 | 3.3 | 3.6 | V |
| BOOST converter output voltage and Power supply voltage range | PVDD | | VBAT | | 7.5 | V |
| Power supply voltage for DVDD | DVDD | | 3 | 3.3 | 3.6 | V |
| Ambient Operating Temperature | $T_a$ | | -25 | 25 | 85 | ℃ |
| DVDD Referenced Digital Input Voltages | $V_I$ | | 0 | | DVDD | V |
| Speaker Load Impedance | $R_L$ | | 2 | 4 | | Ω |

### ● I/O pins

| PARAMETER | Symbol | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Input Logic High threshold for DVDD referenced digital inputs | $V_{IH1}$ | All Digital I/O pins including \FAULT, \SD, SDA, SCL, ADR0, ADR1, MCLK, SCLK, SDIN, LRCK | 70 | | | %DVDD |
| Input Logic LOW threshold for DVDD Referenced Digital Inputs | $V_{IL1}$ | | | | 30 | %DVDD |
| Input Logic HIGH Current Level | $I_{IH1}$ | | | | 15 | uA |
| Input Logic LOW Current Level | $I_{IL1}$ | | | | -15 | uA |
| Output Logic LOW Voltage Level | $V_{OH}$ | | 90 | | | %DVDD |
| Output Logic LOW Voltage Level | $V_{OL}$ | | | | 10 | %DVDD |

### ● Master Clock

| PARAMETER | Symbol | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Allowable MCLK Duty Cycle | $D_{MCLK}$ | | 45 | 50 | 55 | % |
| Supported MCLK Frequencies | $f_{MCLK}$ | Values include: 128, 192, 256, 384, 512. | 128 | | 512 | $f_s$ |
| Pulse duration of MCLK high | $t_{HIGH}$ | | 10.1 | | | ns |
| Pulse duration of MCLK low | $t_{LOW}$ | | 10.1 | | | ns |
| Period of MCLK | $t_{PERIOD}$ | | 20.2 | | | ns |

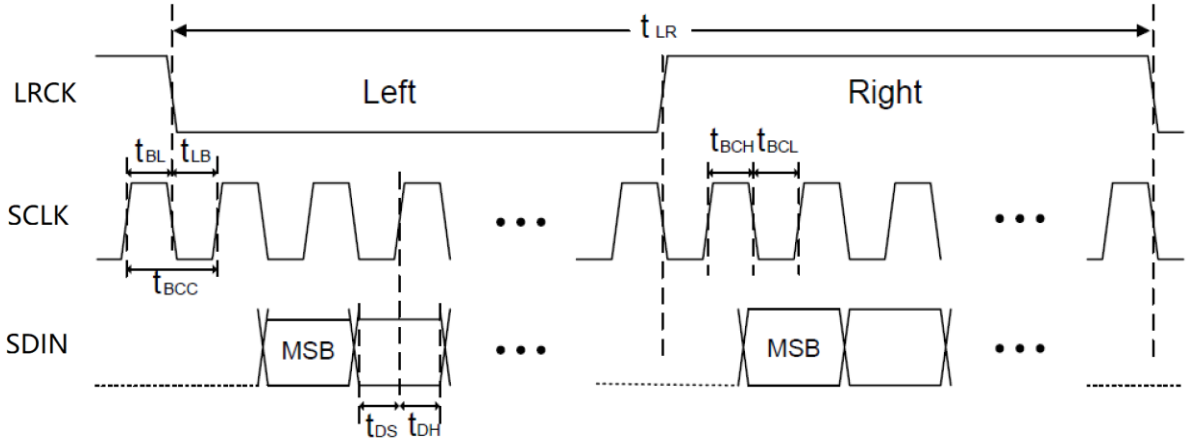



[1] Depending on parts and PCB layout, characteristics may be changed.

[2] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

## Serial Audio Port

| PARAMETER | Symbol | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Allowable SCLK Duty Cycle | $D_{SCLK}$ | | 45 | 50 | 55 | % |
| Supported Input Sample Rates ($1/t_{LR}$) | $f_s$ | | 8 | | 192 | kHz |
| Required LRCK to SCLK Rising Edge | $t_{LB}$ | | 15 | | | ns |
| Required SCLK Rising Edge to LRCK edge | $t_{BL}$ | | 15 | | | ns |
| Supported SCLK Frequencies ($1/t_{BCC}$) for I2S | $F_{SCLK}$ | Values include: 32, 48, 64 | 32 | | 64 | $f_s$ |
| Supported SCLK Frequencies ($1/t_{BCC}$) for TDM | $F_{SCLK}$ | Values include: 128, 256, 512 | 128 | | 512 | $f_s$ |
| SCLK Pulse Width High | $t_{BCL}$ | | | $t_{BCC}/2$ | | |
| SCLK Pulse Width Low | $t_{BCH}$ | | | $t_{BCC}/2$ | | |
| Required SDIN Hold Time after SCLK, Rising Edge | $t_{DH}$ | | 15 | | | ns |
| Required SDIN Setup Time before SCLK Rising Edge | $t_{DS}$ | | 15 | | | ns |




## Boost Converter

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Boost converter output voltage | PVDD | | $V_{BAT}$ | 6.5 | 7.5 | V |
| Boost converter frequency | $f_{SW}$ | | | 410 | | kHz |
| Boost converter input current limit | $I_{LIMTRIP}$ | | | 5 | | A |

## Protection Circuitry

| PARAMETER | Symbol | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| PVDD Overvoltage Error Threshold | $OVE_{RTH}$ | PVDD Rising | | 8.4 | | V |
| PVDD Overvoltage Error Threshold | $OVE_{FTH}$ | PVDD Falling | | 8.2 | | V |
| Overtemperature Error Threshold | $OTE_{TH}$ | | | 150 | | ℃ |
| Overtemperature Error Hysteresis | $OTE_{HYS}$ | | | 15 | | ℃ |
| Overcurrent Error Threshold for Speaker Output | $OCE_{TH}$ | | | 6 | | A |
| Speaker Amplifier Fault Time Out period | $T_{fault}$ | OTE or OCP | | 130 | | ms |

## ● Class D Amplifier

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Class D Channel** $V_{SS}$=0V, $V_{BAT}$ =3.7V, Ta=25ºC, ACF-Off mode, unless otherwise specified | | | | | | |
| Carrier clock frequency | $f_{PWM}$ | default | | 410 | | kHz |
| System Gain | $Av_0$ | default | | 25.5 | | dB |
| Start-up time (power-on or shutdown release) | $t_{STUP}$ | | | 130 | | ms |
| ACF attenuation gain | Aa | | -16 | | 0 | dB |
| Consumption current in shutdown mode (VBAT) | $I_{SD}$ | CTRL=$V_{SS}$ | | 7 | | μA |
| Total Harmonic Distortion plus Noise | THD+N | $P_O$=1.0W, $R_L$=4Ω, f=1kHz | | 0.10 | | % |
| Output Noise | $V_N$ | f=20Hz~20kHz, A weighted, Av=25.5dB | | 220 | | $\mu V_{rms}$ |
| Output offset voltage | $V_{OS}$ | | | ±2 | | mV |
| Quiescent current (VBAT) | $I_{BAT}$ | Input Grounded, PVDD = 6.5V | | 20 | | mA |

| Item | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Class D Channel PVDD = 6.5V** $V_{SS}$=0V, $V_{BAT}$ =3.7V, Ta=25ºC, ACF-Off mode, unless otherwise specified | | | | | | | |
| Output Power | $P_O$ | $R_L$=4Ω | $V_{BAT}$=3.7V, f=1kHz, THD+N=10% | | 5.5 | | W |
| | | $R_L$=3Ω | | | 7 | | |
| | | $R_L$=2Ω+33uH | | | 9 | | |
| | | $R_L$=8Ω | | | 3.1 | | |
| | | $R_L$=4Ω | $V_{BAT}$=3.7V, f=1kHz, THD+N=1% | | 4.4 | | |
| | | $R_L$=3Ω, | | | 5.5 | | |
| | | $R_L$=2Ω+33uH | | | 5.5 | | |
| | | $R_L$=8Ω | | | 2.5 | | |
| Efficiency (Class D + Boost) | η | $V_{BAT}$=4.2V, $R_L$=4Ω, THD+N = 10% | | | 75 | | % |
| | | $V_{BAT}$=4.2V, $R_L$=3Ω, THD+N = 10% | | | 70 | | % |
| | | $V_{BAT}$=4.2V, $R_L$=2Ω+33uH, THD+N = 10% | | | 66 | | % |
| | | $V_{BAT}$=4.2V, $R_L$=8Ω+33uH, THD+N = 10% | | | 80 | | % |

| Item | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Class D Channel PVDD = 7.0V** $V_{SS}$=0V, $V_{BAT}$ =3.7V, Ta=25ºC, ACF-Off mode, unless otherwise specified | | | | | | | |
| Output Power | $P_O$ | $R_L$=4Ω | $V_{BAT}$=3.7V, f=1kHz, THD+N=10% | | 6.2 | | W |
| | | $R_L$=3Ω | | | 7.6 | | |
| | | $R_L$=2Ω+33uH | | | 9.5 | | |
| | | $R_L$=4Ω | $V_{BAT}$=3.7V, f=1kHz, THD+N=1% | | 5.1 | | |
| | | $R_L$=3Ω, | | | 6.2 | | |
| | | $R_L$=2Ω+33uH | | | 7.5 | | |
| Efficiency (Class D + Boost) | η | $V_{BAT}$=4.2V, $R_L$=4Ω, THD+N = 10% | | | 73 | | % |
| | | $V_{BAT}$=4.2V, $R_L$=3Ω, THD+N = 10% | | | 69 | | % |
| | | $V_{BAT}$=4.2V, $R_L$=2Ω+33uH, THD+N = 10% | | | 66 | | % |

| Item | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Class D Channel PVDD = 7.5V** $V_{SS}$=0V, $V_{BAT}$ =3.7V, Ta=25ºC, ACF-Off mode, unless otherwise specified | | | | | | | |
| Output Power | $P_O$ | $R_L$=4Ω | $V_{BAT}$=3.7V, f=1kHz, THD+N=10% | | 7 | | W |
| | | $R_L$=3Ω | | | 9 | | |
| | | $R_L$=2Ω+33uH | | | 11 | | |
| | | $R_L$=4Ω | $V_{BAT}$=3.7V, f=1kHz, THD+N=1% | | 5.5 | | |
| | | $R_L$=3Ω, | | | 7 | | |
| | | $R_L$=2Ω+33uH | | | 8.8 | | |
| Efficiency (Class D + Boost) | η | $V_{BAT}$=4.2V, $R_L$=4Ω, THD+N = 10% | | | 72 | | % |
| | | $V_{BAT}$=4.2V, $R_L$=3Ω, THD+N = 10% | | | 68 | | % |
| | | $V_{BAT}$=4.2V, $R_L$=2Ω+33uH, THD+N = 10% | | | 66 | | % |

## ● Class AB Amplifier

| **Class AB Channel** [1] $V_{SS}$=0V, $V_{BAT}$ =3.6V, $R_{IN}$ = 0ohm, Ta=25ºC, unless otherwise specified | | | | | | | |
|---|---|---|---|---|---|---|---|
| Output Power | $P_O$ | $R_L$=4Ω, $V_{BAT}$=3.6V | f=1kHz, THD+N=10% | | 1.3 | | W |
| | | $R_L$=4Ω, $V_{BAT}$=4.2V | | | 1.8 | | |
| | | $R_L$=4Ω, $V_{BAT}$=5.0V | | | 2.65 | | W |
| | | $R_L$=4Ω, $V_{BAT}$=3.6V | f=1kHz, THD+N=1% | | 1.0 | | W |
| | | $R_L$=4Ω, $V_{BAT}$=4.2V | | | 1.5 | | W |
| | | $R_L$=4Ω, $V_{BAT}$=5.0V | | | 2.1 | | W |
| Total Harmonic Distortion plus Noise | THD+N | $P_O$=0.01W | $R_L$=4Ω, f=1kHz | | 0.1 | | % |
| | | $P_O$=0.1W | | | 0.09 | | % |
| Output Noise | $V_N$ | f=20Hz~20kHz, A weighted, Av = 19dB | | | 200 | | $\mu V_{rms}$ |
| Output offset voltage | $V_{OS}$ | | | | ±4 | | mV |
| Efficiency | η | $R_L$=4Ω+22uH, THD+N = 10% | | | 70 | | % |
| | | $R_L$=8Ω+33uH, THD+N = 10% | | | 74.5 | | % |
| Quiescent current (VBAT) | $I_{BAT}$ | Input Grounded | | | 20 | | mA |
| System Gain | $Av_0$ | Default | | | 19 | | dB |
| Start-up time (power-on, shutdown release, or switch from Class D to Class AB) | $t_{STUP}$ | | | | 130 | | ms |

[1] In Class AB amplifier mode, boost converter is shutdown automatically. Due to the schottky rectifier, the voltage of PVDD terminal can be lower than VBAT, depending on the forward voltage of the rectifier $V_F$.

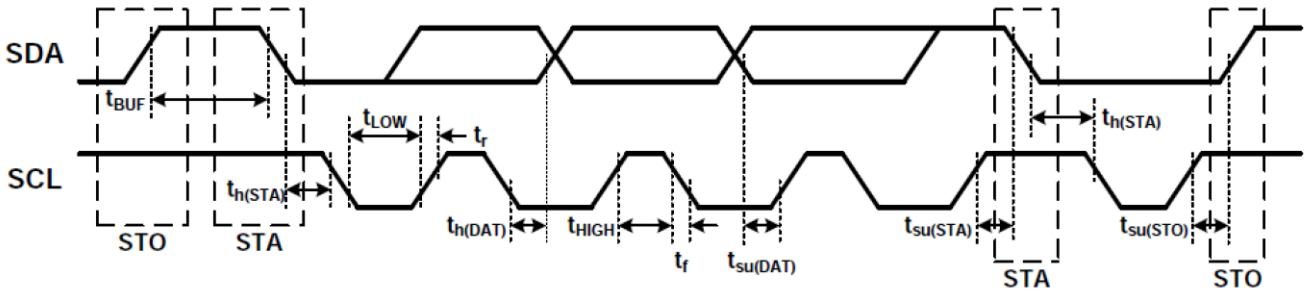
## ● DVDD & AVDD current consumption

TA = 25°, DVDD = AVDD = 3.3V, fs = 48kHz, (unless otherwise noted)

| PARAMETER | Symbol | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Quiescent current in DVDD+AVDD | $I_{DVDD+AVDD}$ | fs=48kHz MCLK=128*fs | | 4.5 | | mA |
| | | fs=48kHz MCLK=256*fs | | 5.3 | | mA |
| | | fs=48kHz MCLK=512*fs | | 5.5 | | mA |
| | | fs=32kHz MCLK=128*fs | | 6.7 | | mA |
| | | fs=32kHz MCLK=256*fs | | 8.3 | | mA |
| | | fs=32kHz MCLK=512*fs | | 8.8 | | mA |
| DVDD+AVDD current consumption in sleep mode | $I_{DVDD+AVDD\_SLEEP}$ | SLEEP = H, fs=48kHz MCLK=256*fs | | 3.0 | | mA |
| | | SLEEP = H, fs=32kHz MCLK=256*fs | | 3.5 | | mA |
| DVDD+AVDD current consumption in SD mode | $I_{DVDD+AVDD\_SD}$ | \SD = L, No clock | | 120 | | uA |

## ● I²C Control Port

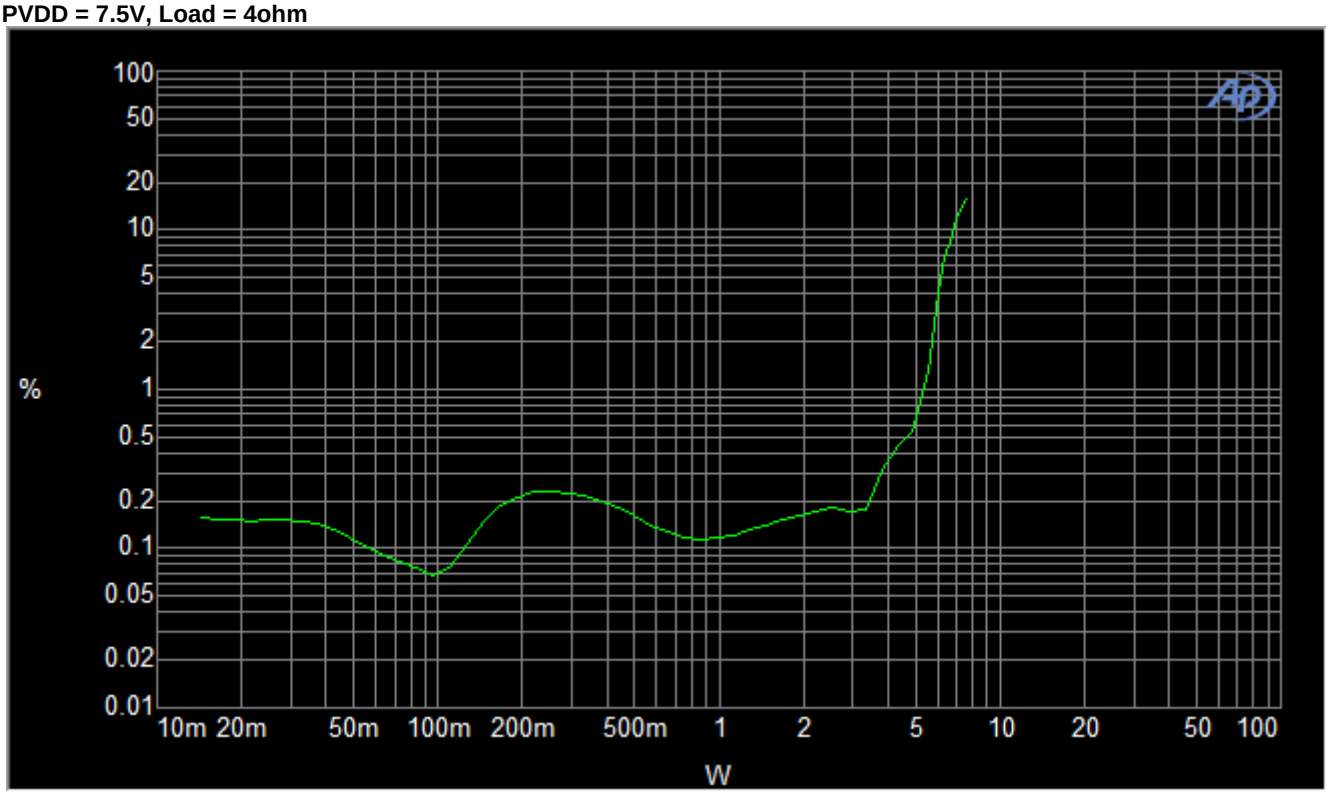
| PARAMETER | Symbol | Standard-Mode | | | Fast-Mode | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Allowable Load Capacitance for Each I²C Line | $C_b$ | | | 400 | | | 400 | pF |
| Support SCL frequency | $f_{SCL}$ | | | 100 | | | 400 | kHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{h(STA)}$ | 4 | | | 0.6 | | | us |
| Required Pulse Duration, SCL HIGH | $t_{HIGH}$ | 4 | | | 0.6 | | | us |
| Required Pulse Duration, SCL LOW | $t_{LOW}$ | 4.7 | | | 1.3 | | | us |
| Setup time for a repeated START condition | $t_{su(STA)}$ | 4.7 | | | 0.6 | | | us |
| Data hold time | $t_{h(DAT)}$ | 0 | | 3.45 | 0 | | 0.9 | us |
| Setup Time, SDA to SCL | $t_{su(DAT)}$ | 250 | | | 100 | | | ns |
| Rise Time, SCL | $T_{r\_SCL}$ | | | 1000 | | | 300 | ns |
| Rise Time, SDA | $T_{r\_SDA}$ | | | $1/(4*f_{scl})$-0.25 | | | $1/(4*f_{scl})$-0.25 | us |
| Fall Time, SCL and SDA | $T_f$ | | | 300 | | | 300 | ns |
| Setup Time, SCL to STOP condition | $t_{su(STO)}$ | 4 | | | 0.6 | | | us |
| Bus Free time between STOP and START conditions | $t_{BUF}$ | 4.7 | | | 1.3 | | | us |



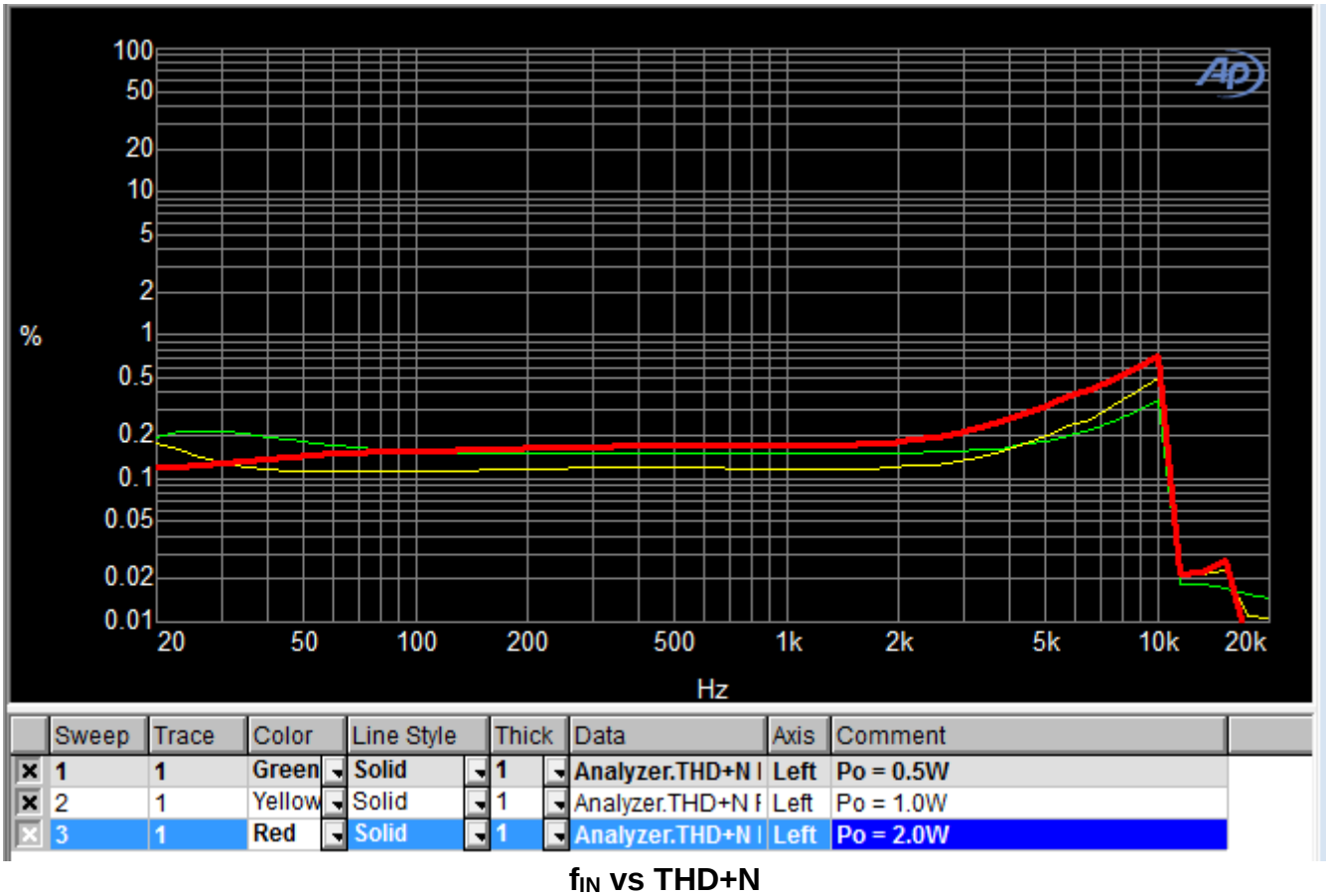
## ■ TYPICAL OPERATING CHARACTERISTICS

**Class D Channel**
Condition: Class D mode, $V_{BAT}$ = 3.7V, $f_{IN}$ = 1kHz, ACF off, unless otherwise specified

**PVDD = 7.5V, Load = 4ohm**

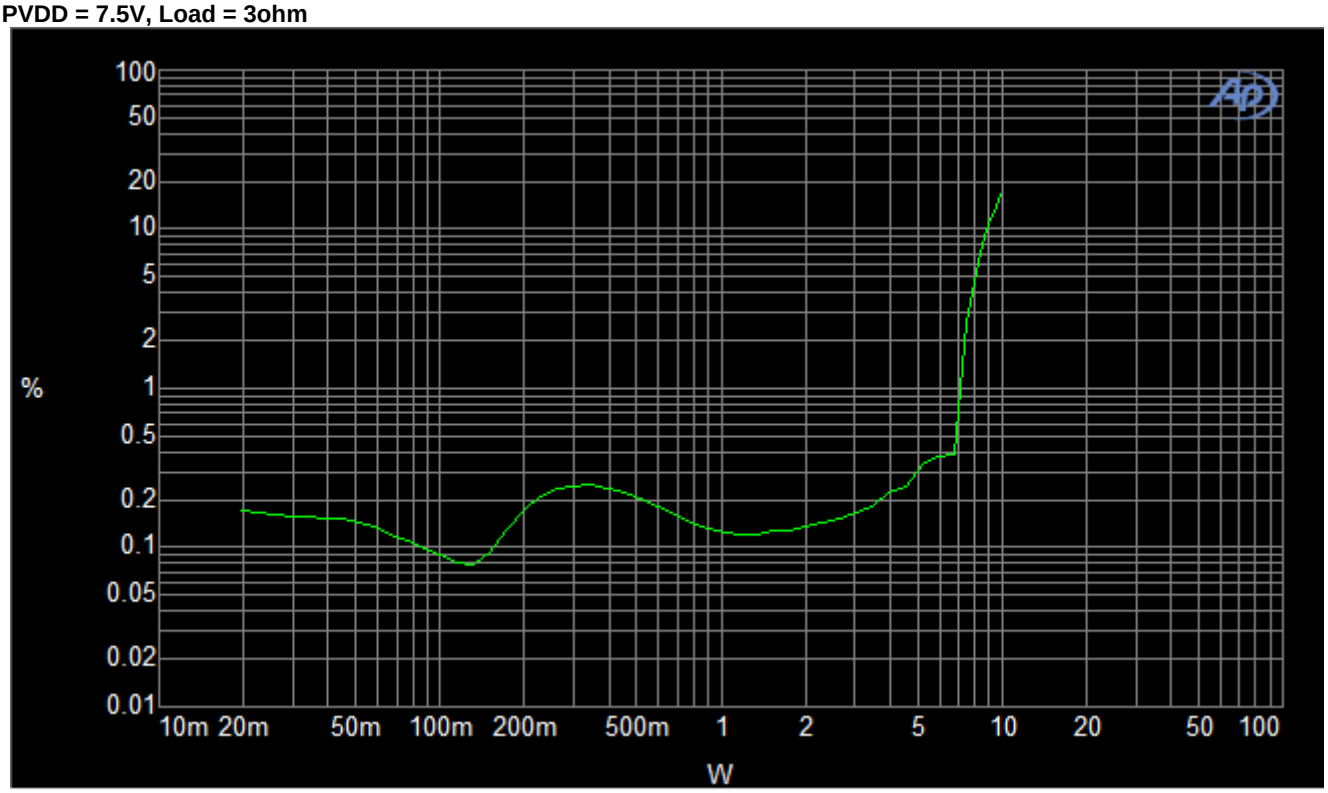



**Output Power vs THD+N**

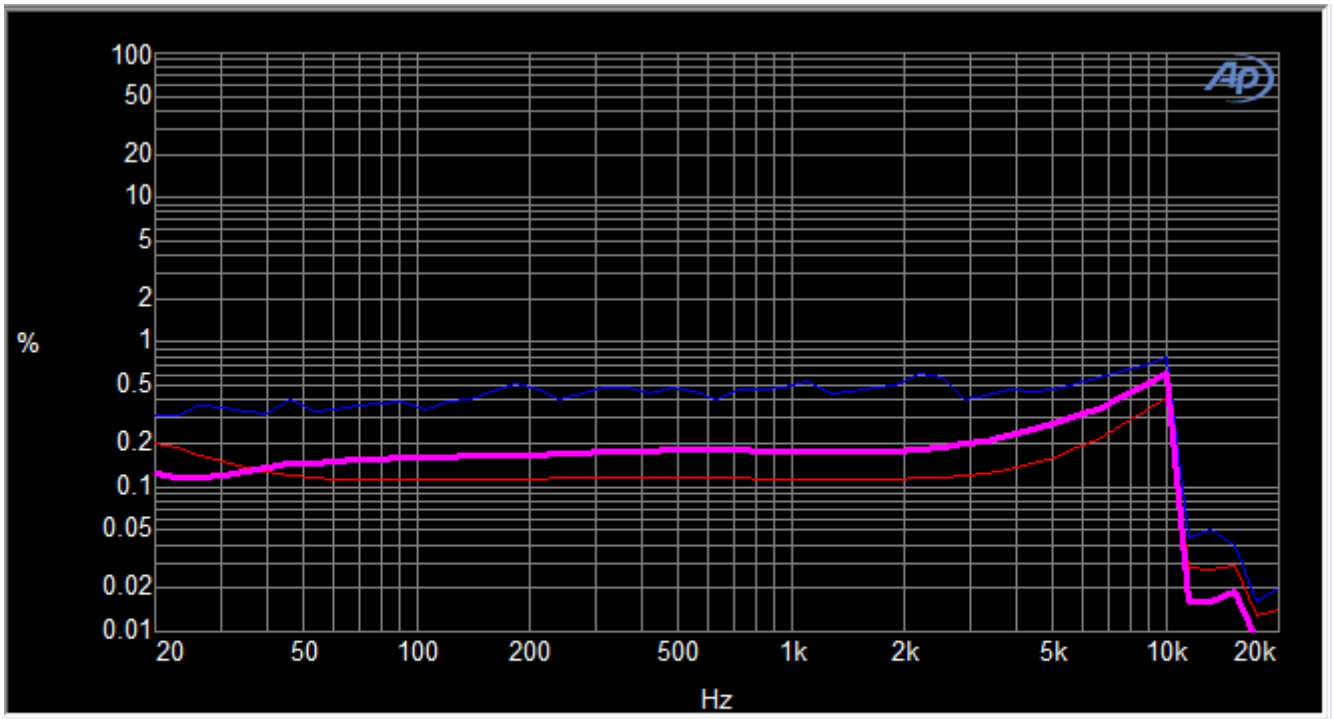



**$f_{IN}$ vs THD+N**

PVDD = 7.5V, Load = 3ohm



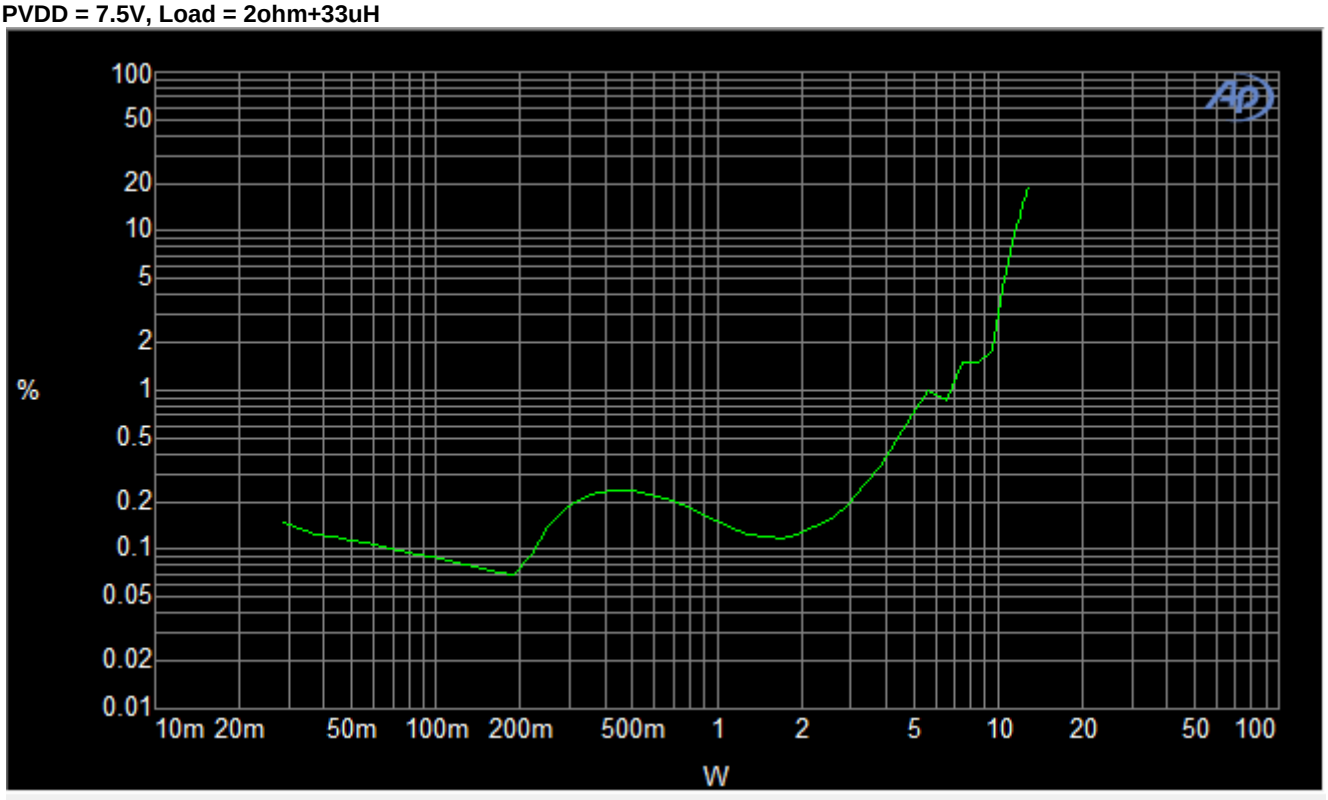

**Output Power vs THD+N**



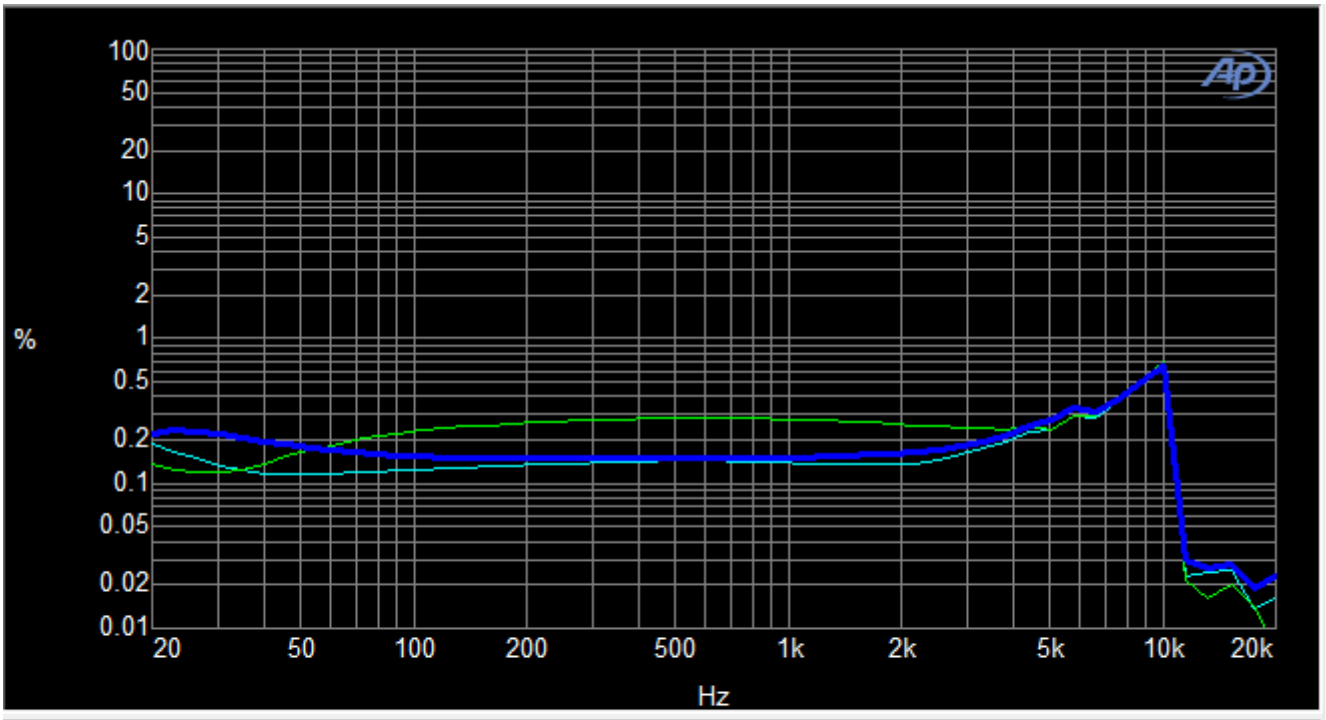

| | Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|---|
| ✕ | 1 | 1 | Red | Solid | 1 | Analyzer.THD+N I | Left | Po = 1W |
| ✕ | 2 | 1 | Mager | Solid | 1 | Analyzer.THD+N I | Left | Po = 2W |
| ✕ | 3 | 1 | Blue | Solid | 1 | Analyzer.THD+N I | Left | Po = 3W |

**$f_{IN}$ vs THD+N**

**PVDD = 7.5V, Load = 2ohm+33uH**



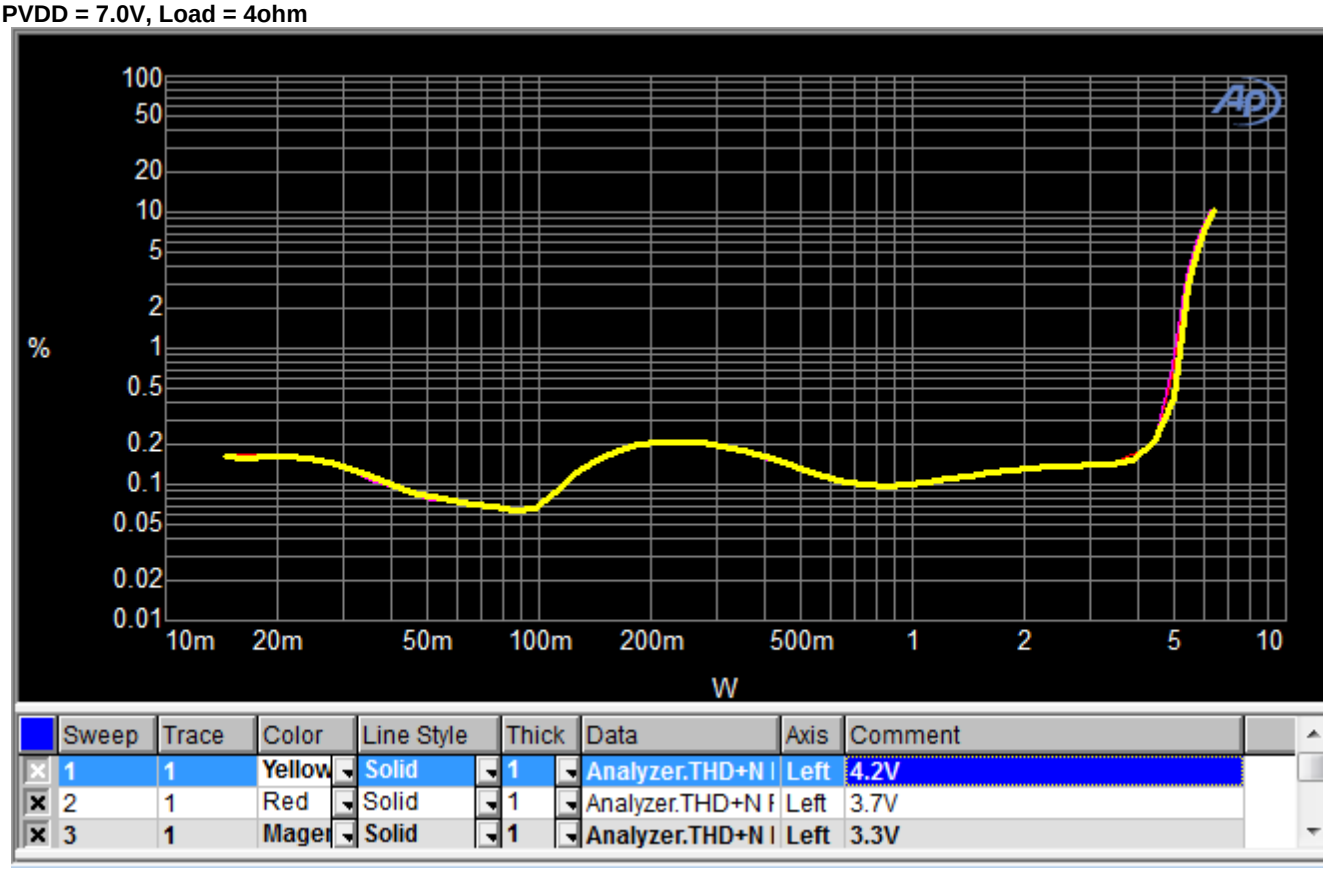

**Output Power vs THD+N**



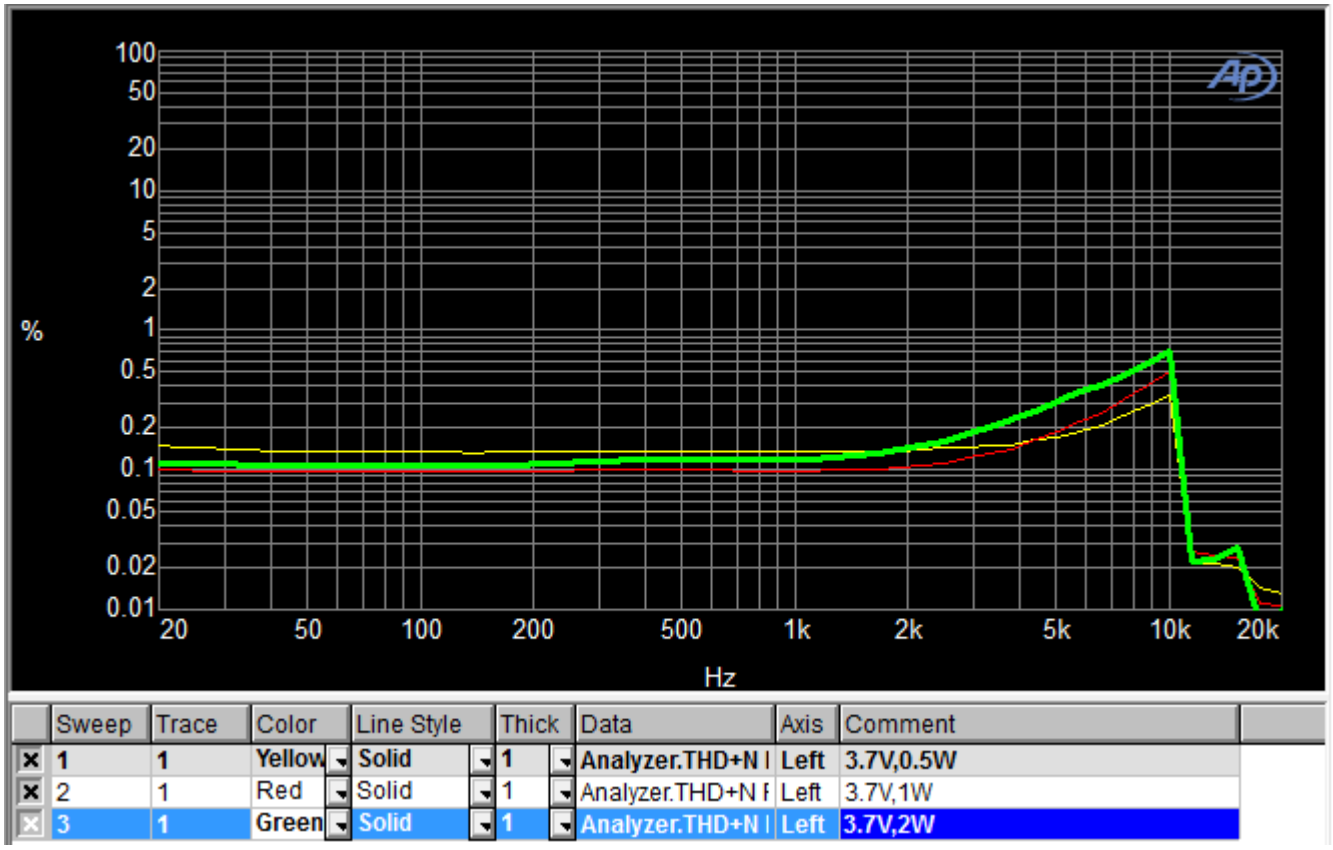

| | Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|---|
| ☒ | 1 | 1 | Blue | Solid | 1 | Analyzer.THD+N I | Left | Po = 1W |
| ☒ | 2 | 1 | Cyan | Solid | 1 | Analyzer.THD+N F | Left | Po = 2W |
| ☒ | 3 | 1 | Green | Solid | 1 | Analyzer.THD+N I | Left | Po = 3W |

**$f_{IN}$ vs THD+N**

**PVDD = 7.0V, Load = 4ohm**

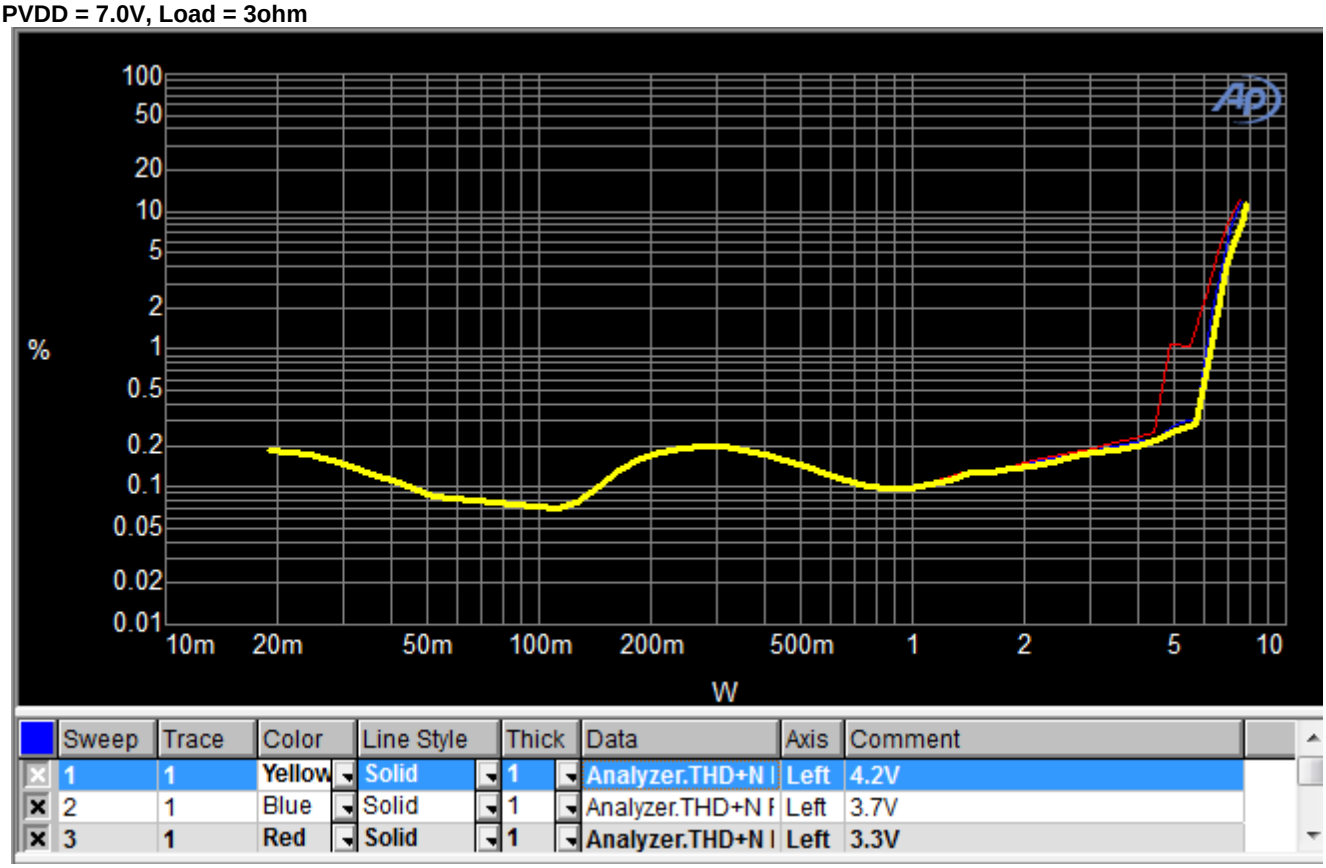



**Output Power vs THD+N**

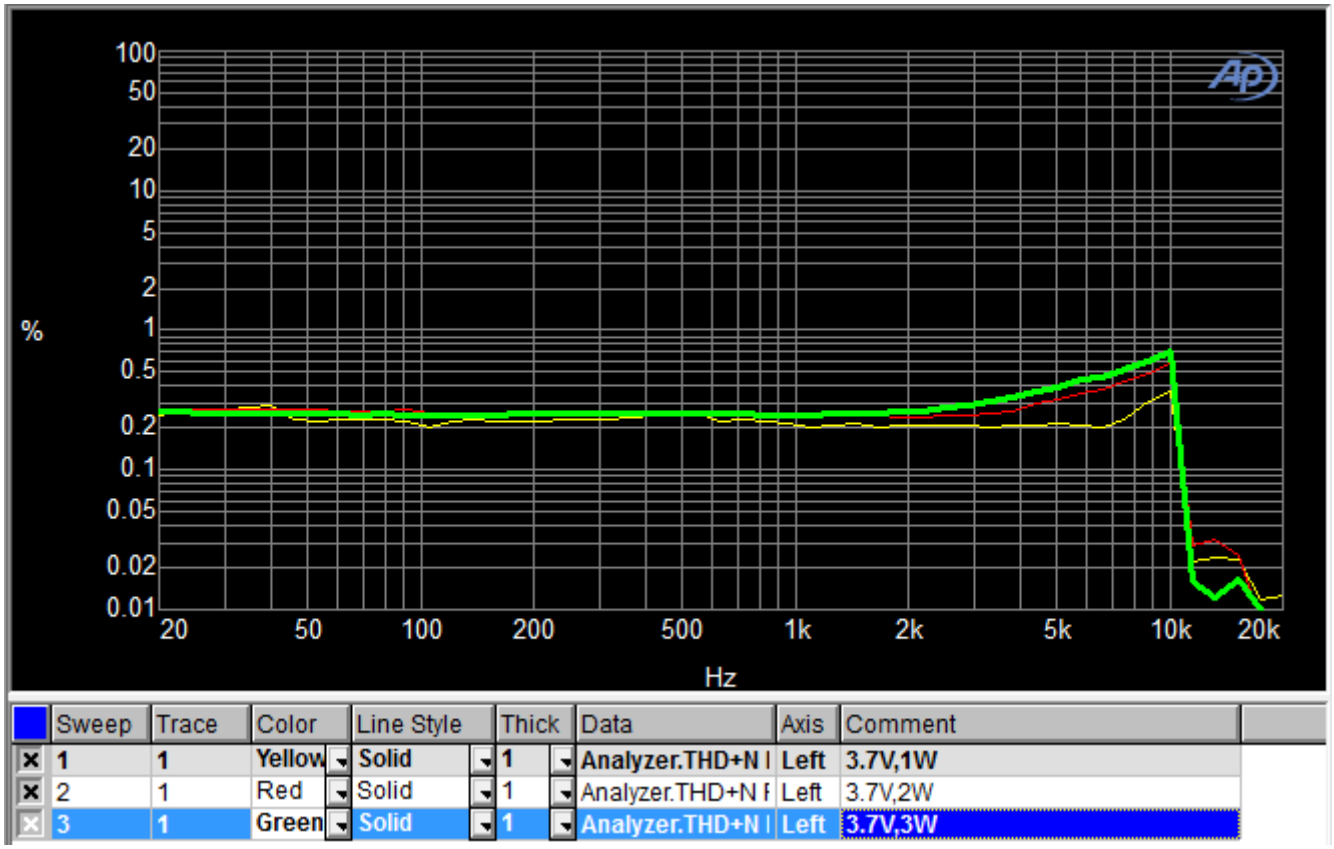



**$f_{IN}$ vs THD+N**

**PVDD = 7.0V, Load = 3ohm**

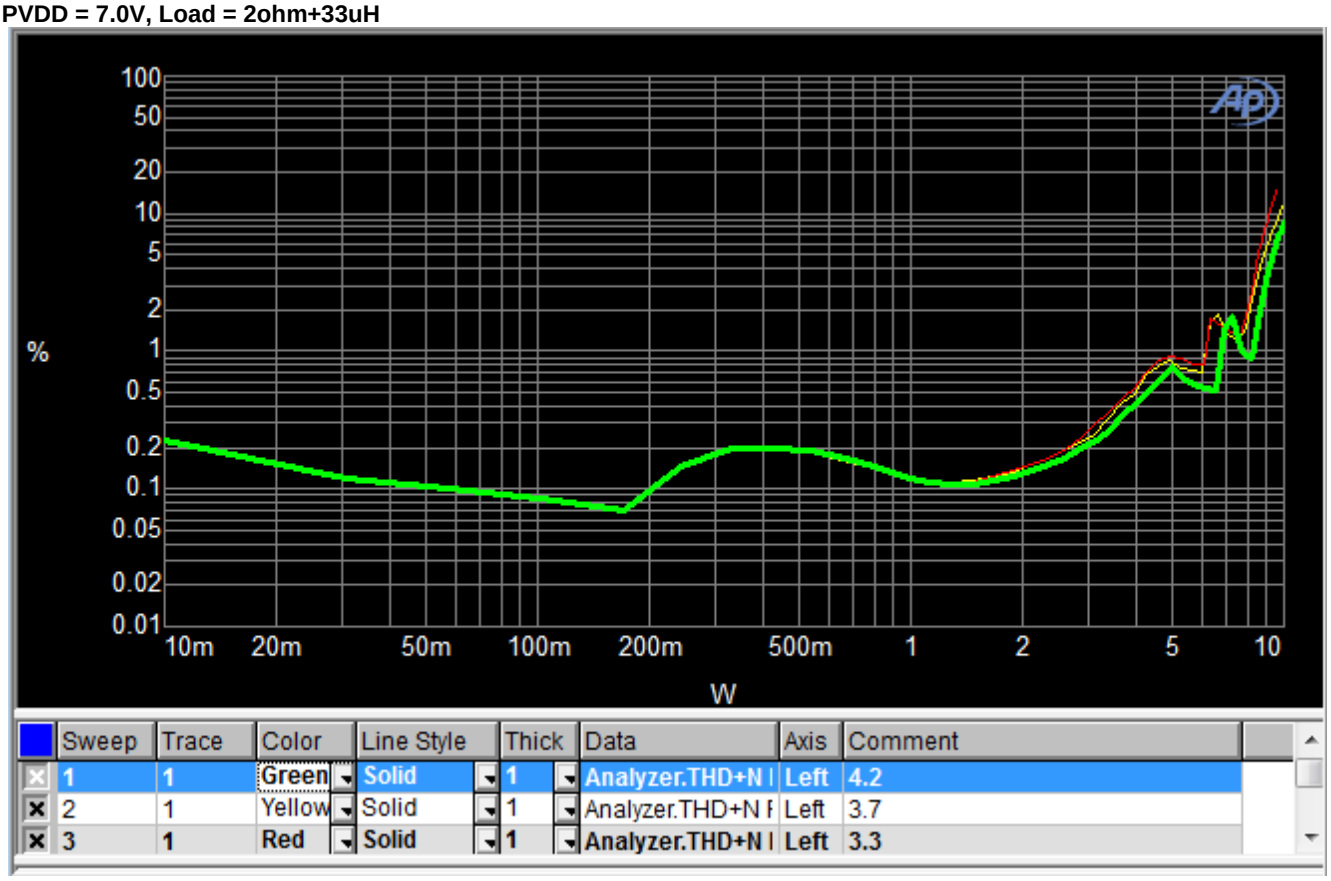



**Output Power vs THD+N**

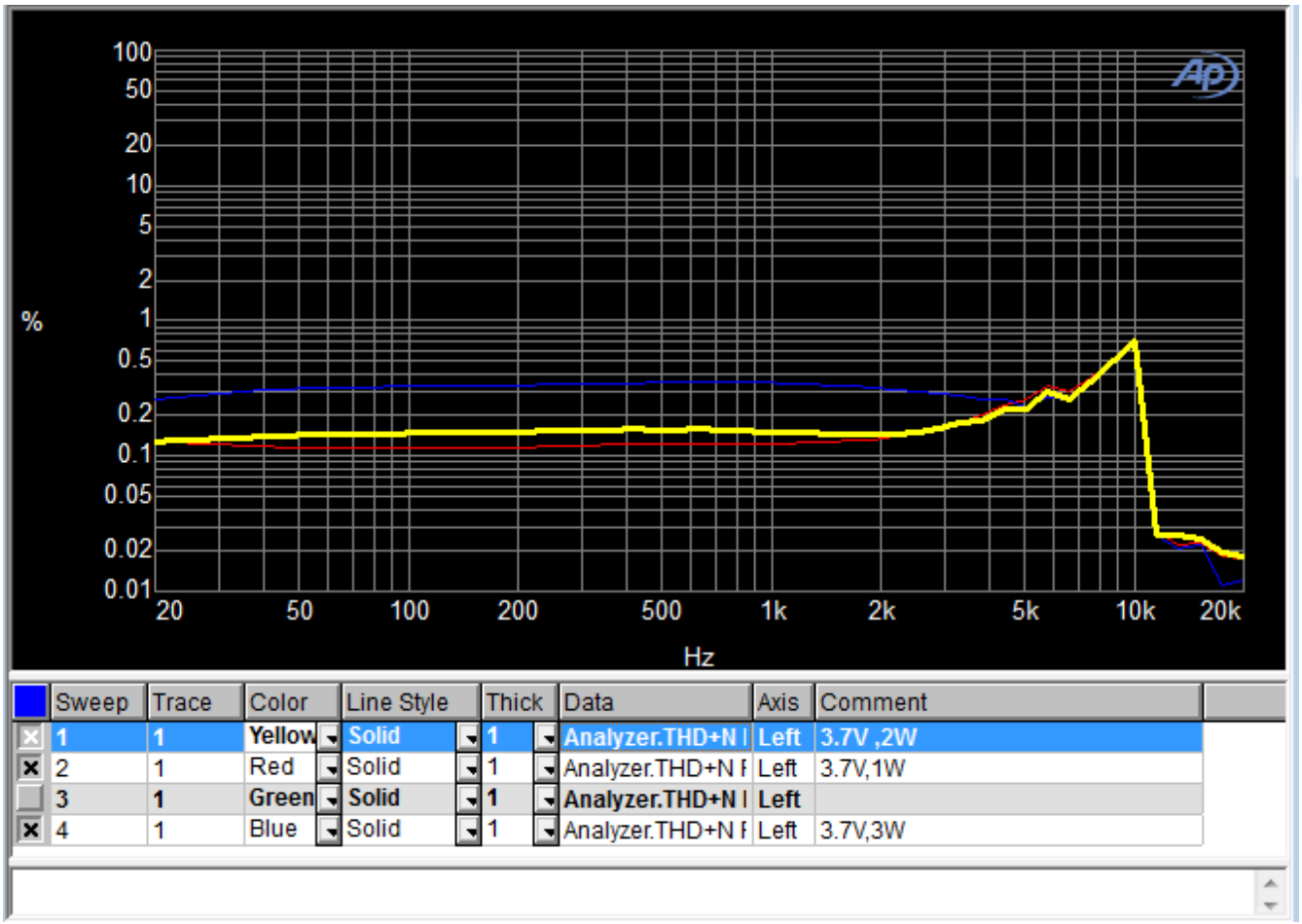



**$f_{IN}$ vs THD+N**

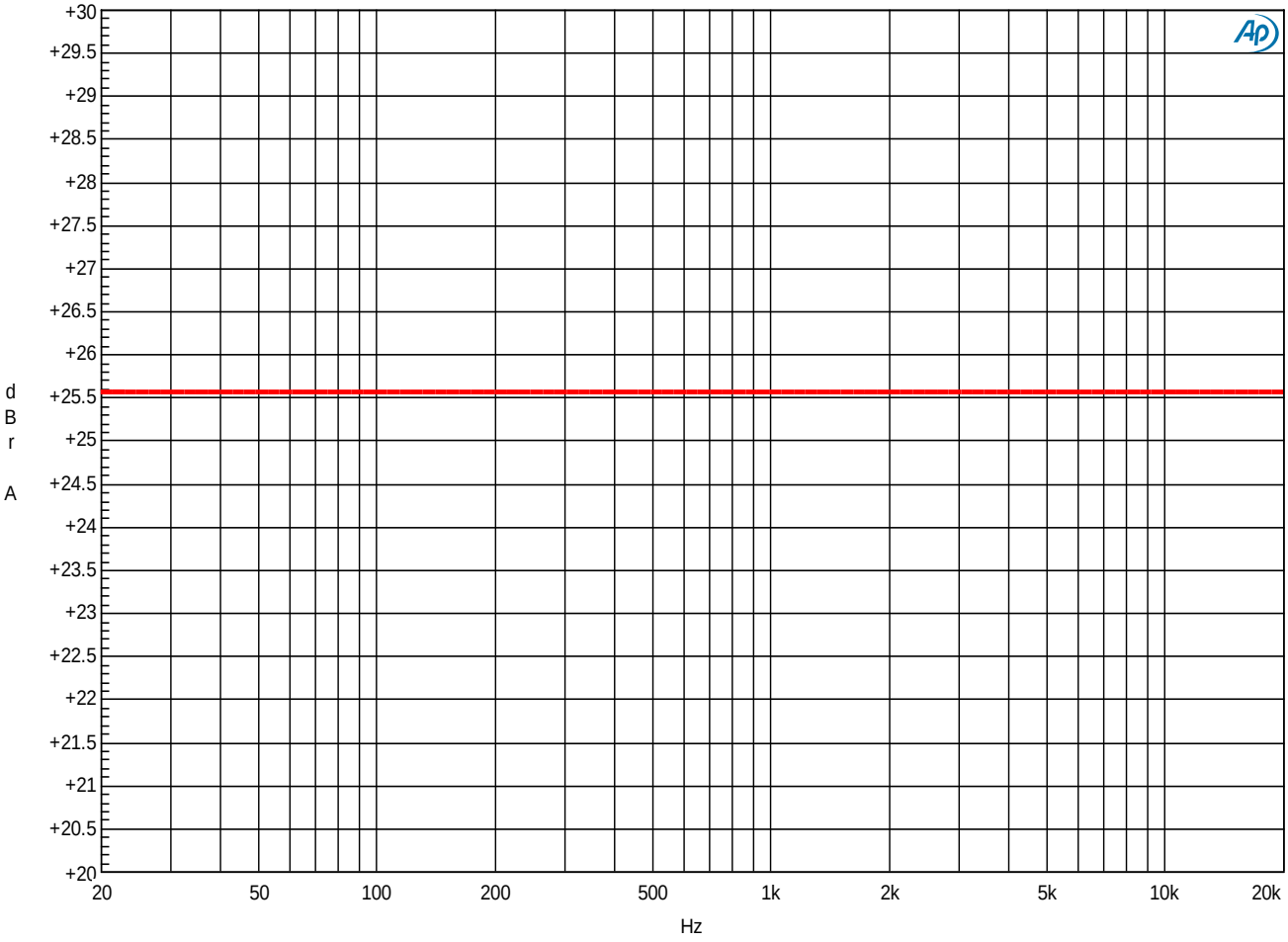
**PVDD = 7.0V, Load = 2ohm+33uH**




**Output Power vs THD+N**



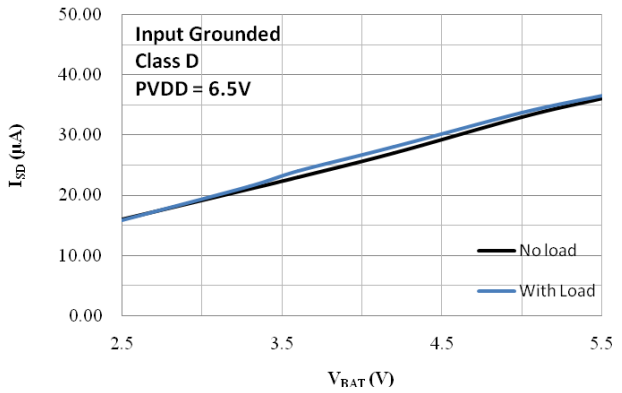

**$f_{IN}$ vs THD+N**



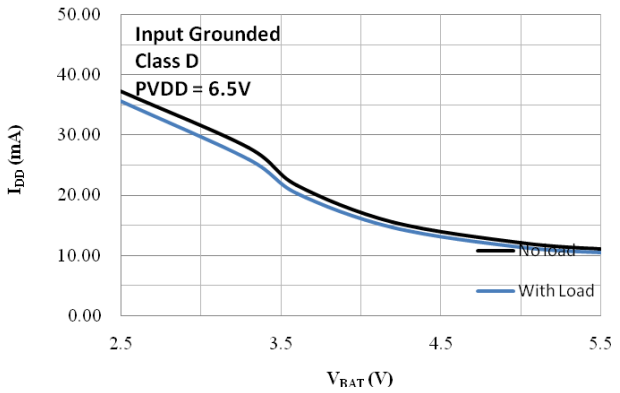

| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Red | Solid | 3 | Analyzer.Level A | Left | f vs gain |

Frequency Respond.ats2

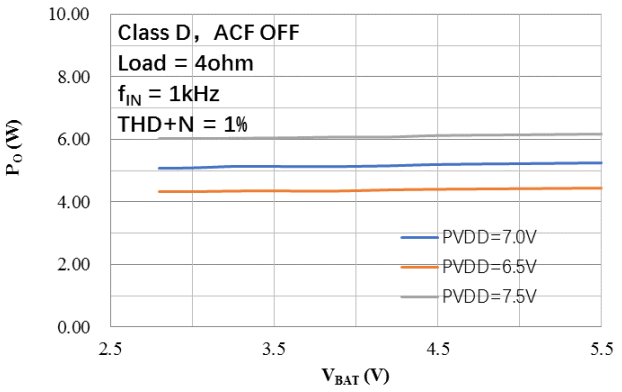
## $V_{BAT}$ vs $I_{SD}$



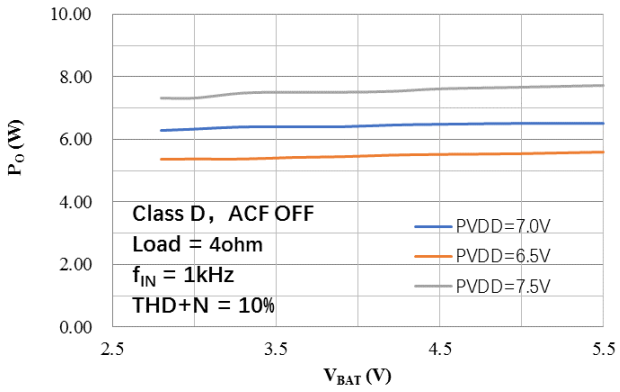

## $V_{BAT}$ vs $I_{DD}$



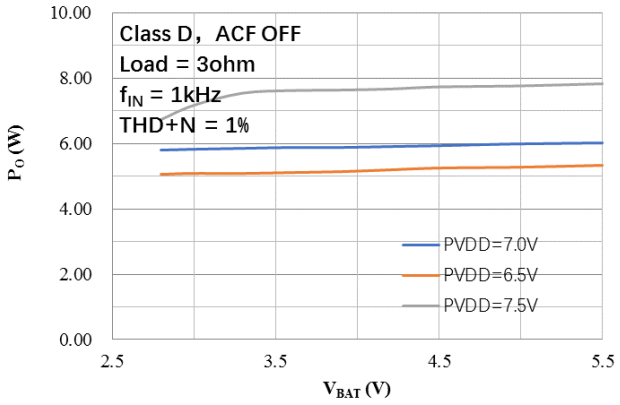

## $V_{BAT}$ vs $P_O$



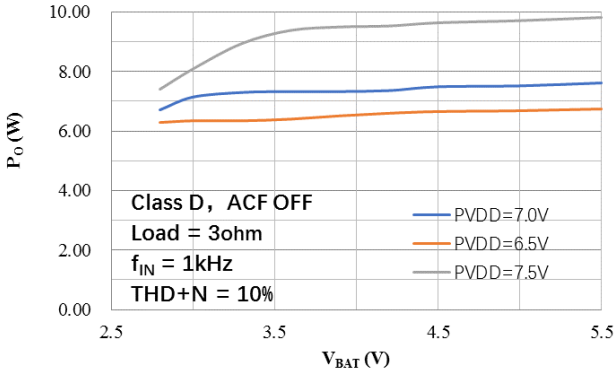

## $V_{BAT}$ vs $P_O$



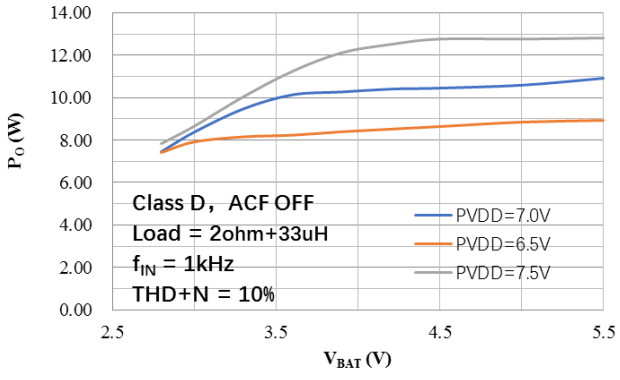

## $V_{BAT}$ vs $P_O$

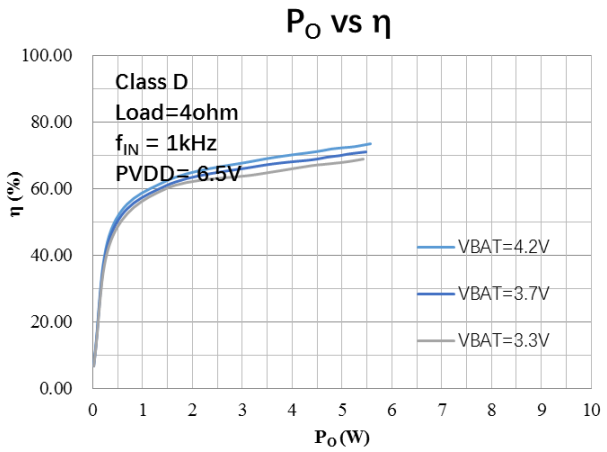


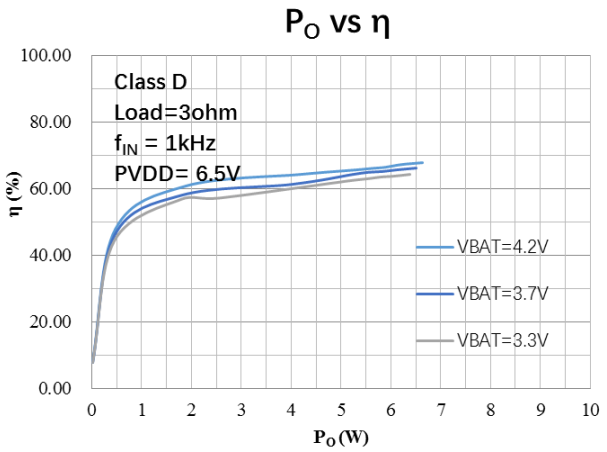

## $V_{BAT}$ vs $P_O$

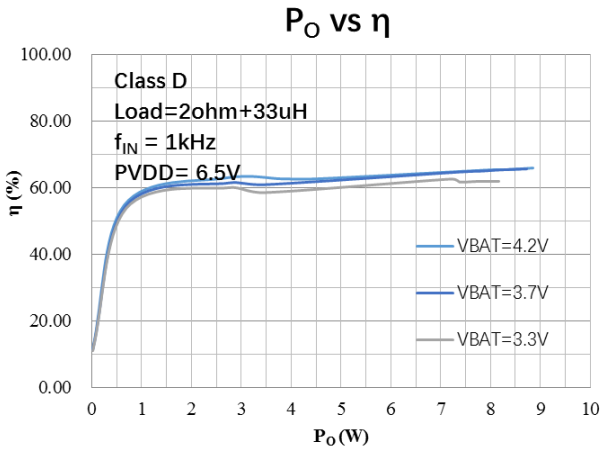


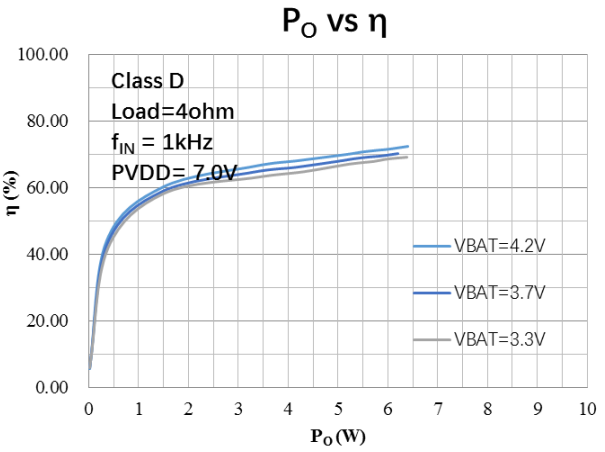

## $V_{BAT}$ vs $P_O$

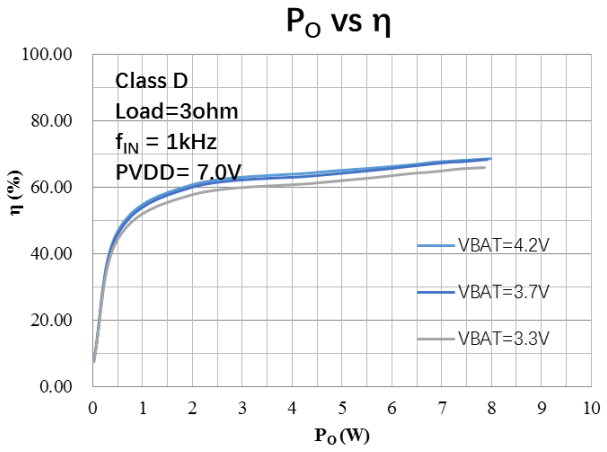


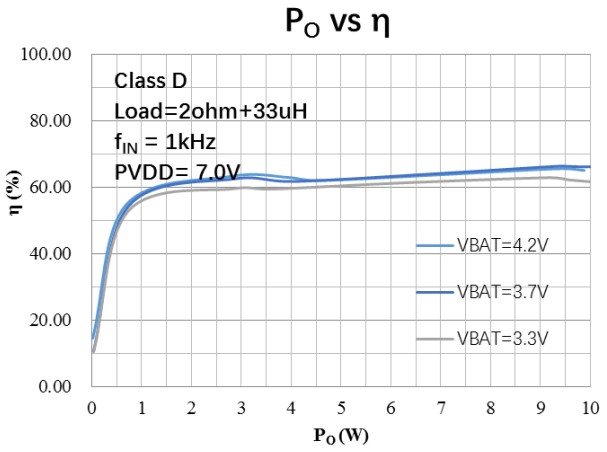

Po vs η
Class D
Load=4ohm
fIN = 1kHz
PVDD= 6.5V
VBAT=4.2V
VBAT=3.7V
VBAT=3.3V
η (%)
Po (W)

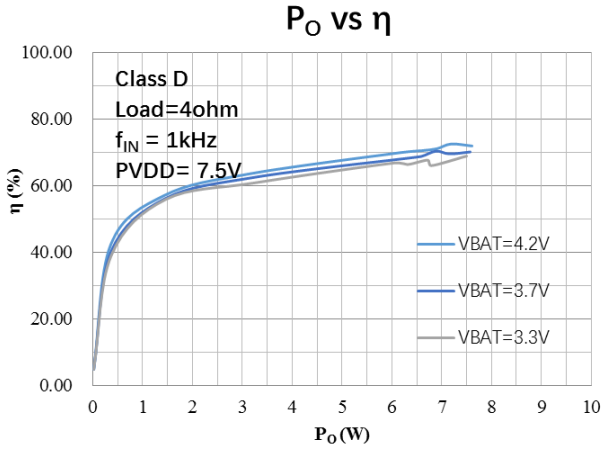

Po vs η
Class D
Load=3ohm
fIN = 1kHz
PVDD= 6.5V
VBAT=4.2V
VBAT=3.7V
VBAT=3.3V
η (%)
Po (W)

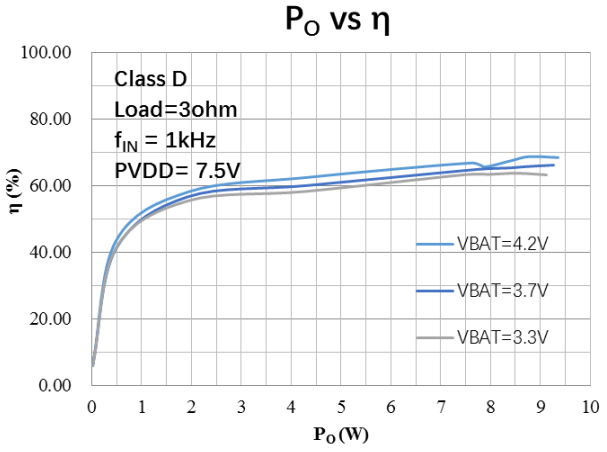

Po vs η
Class D
Load=2ohm+33uH
fIN = 1kHz
PVDD= 6.5V
VBAT=4.2V
VBAT=3.7V
VBAT=3.3V
η (%)
Po (W)

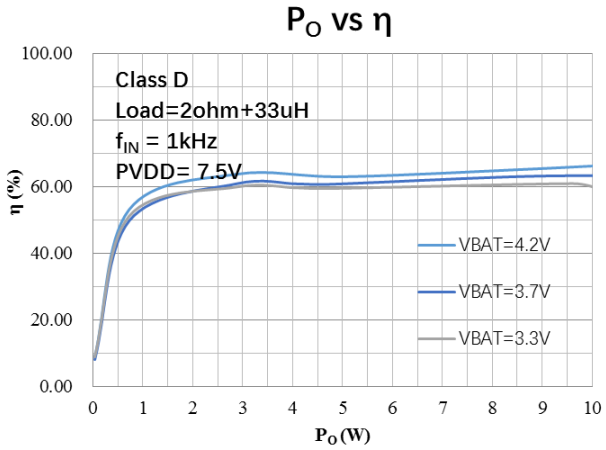

Po vs η
Class D
Load=4ohm
fIN = 1kHz
PVDD= 7.0V
VBAT=4.2V
VBAT=3.7V
VBAT=3.3V
η (%)
Po (W)


Po vs η
Class D
Load=3ohm
fIN = 1kHz
PVDD= 7.0V
VBAT=4.2V
VBAT=3.7V
VBAT=3.3V
η (%)
Po (W)


Po vs η
Class D
Load=2ohm+33uH
fIN = 1kHz
PVDD= 7.0V
VBAT=4.2V
VBAT=3.7V
VBAT=3.3V
η (%)
Po (W)


Po vs η
Class D
Load=4ohm
fIN = 1kHz
PVDD= 7.5V
VBAT=4.2V
VBAT=3.7V
VBAT=3.3V
η (%)
Po (W)

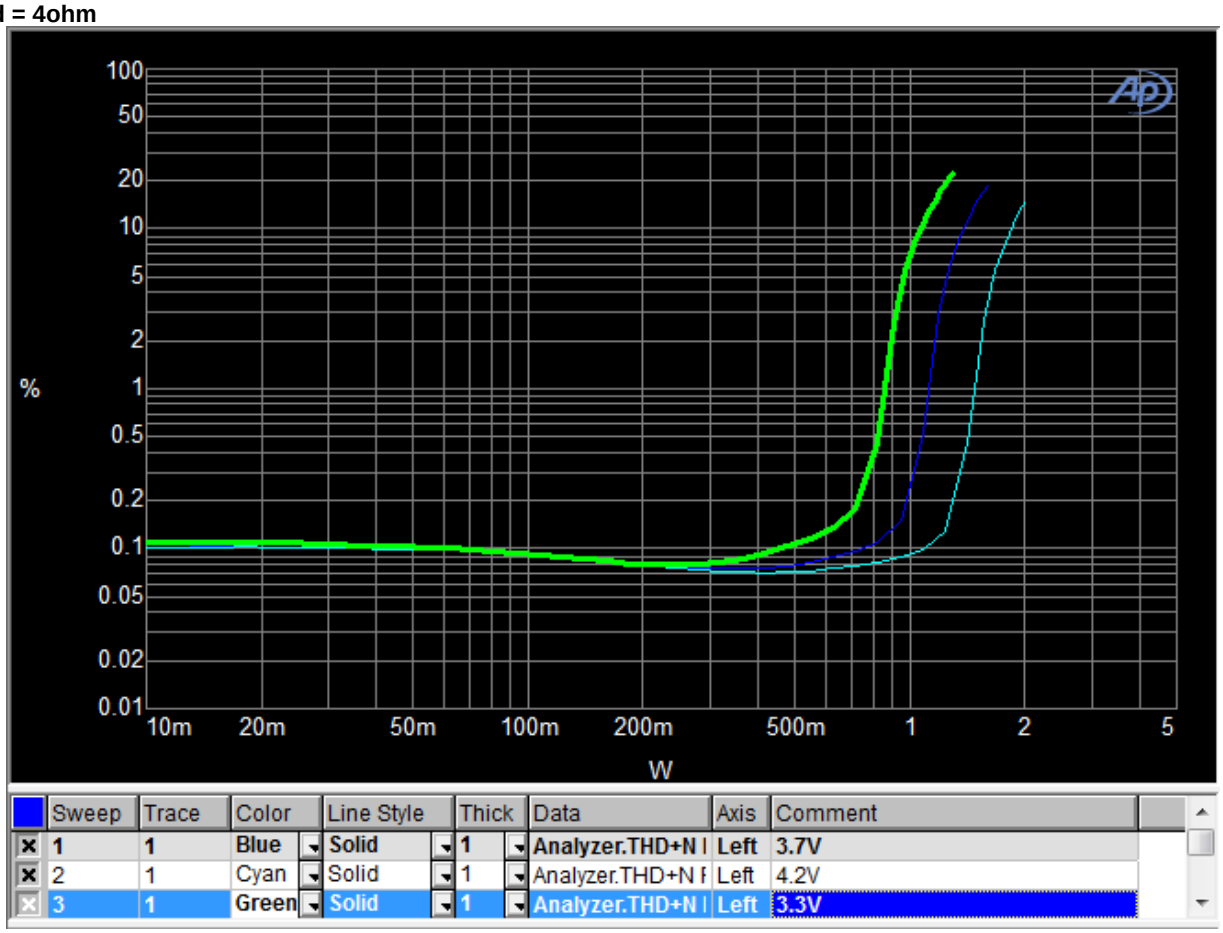

Po vs η
Class D
Load=3ohm
fIN = 1kHz
PVDD= 7.5V
VBAT=4.2V
VBAT=3.7V
VBAT=3.3V
η (%)
Po (W)


Po vs η
Class D
Load=2ohm+33uH
fIN = 1kHz
PVDD= 7.5V
VBAT=4.2V
VBAT=3.7V
VBAT=3.3V
η (%)
100.00
80.00
60.00
40.00
20.00
0.00
0
1
2
3
4
5
6
7
8
9
10
Po (W)

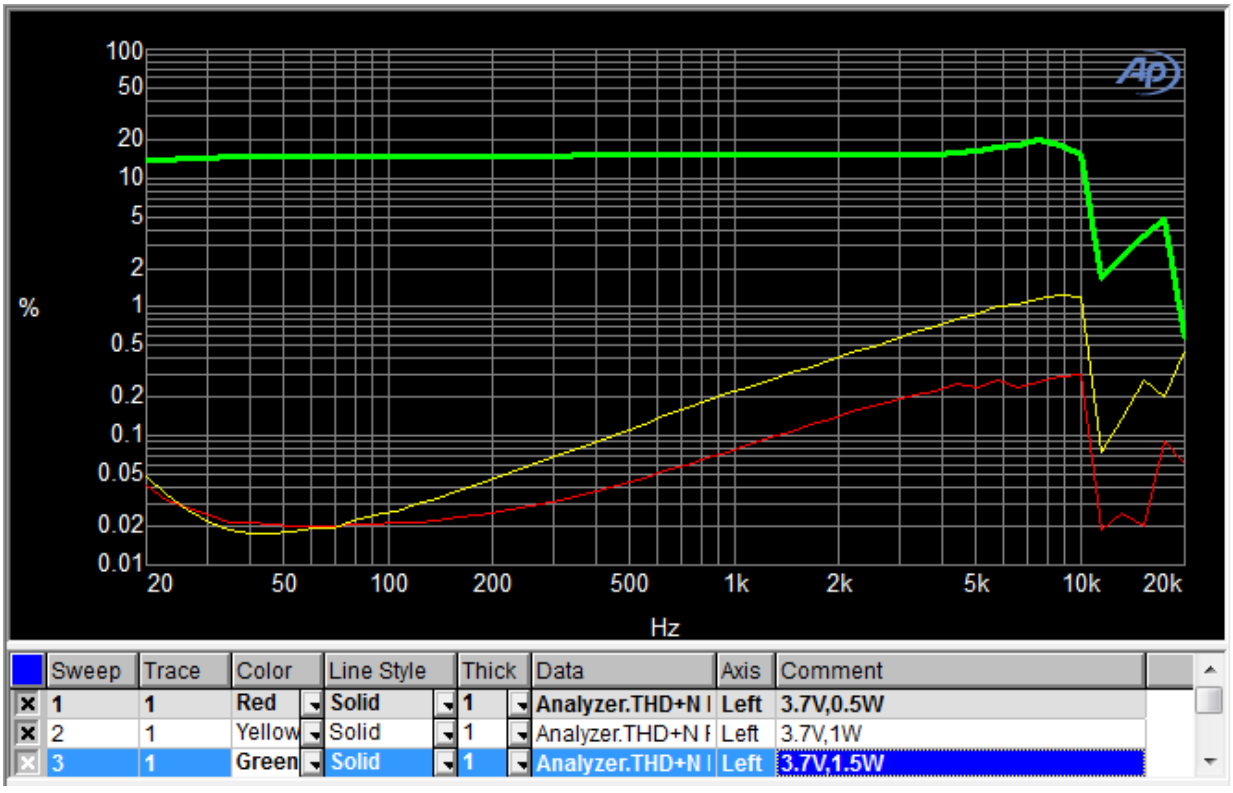
**Class AB Channel**

Condition: Class AB mode, $V_{BAT}$ = 3.7V, $f_{IN}$ = 1kHz, Load = 4ohm, unless otherwise specified

**Load = 4ohm**

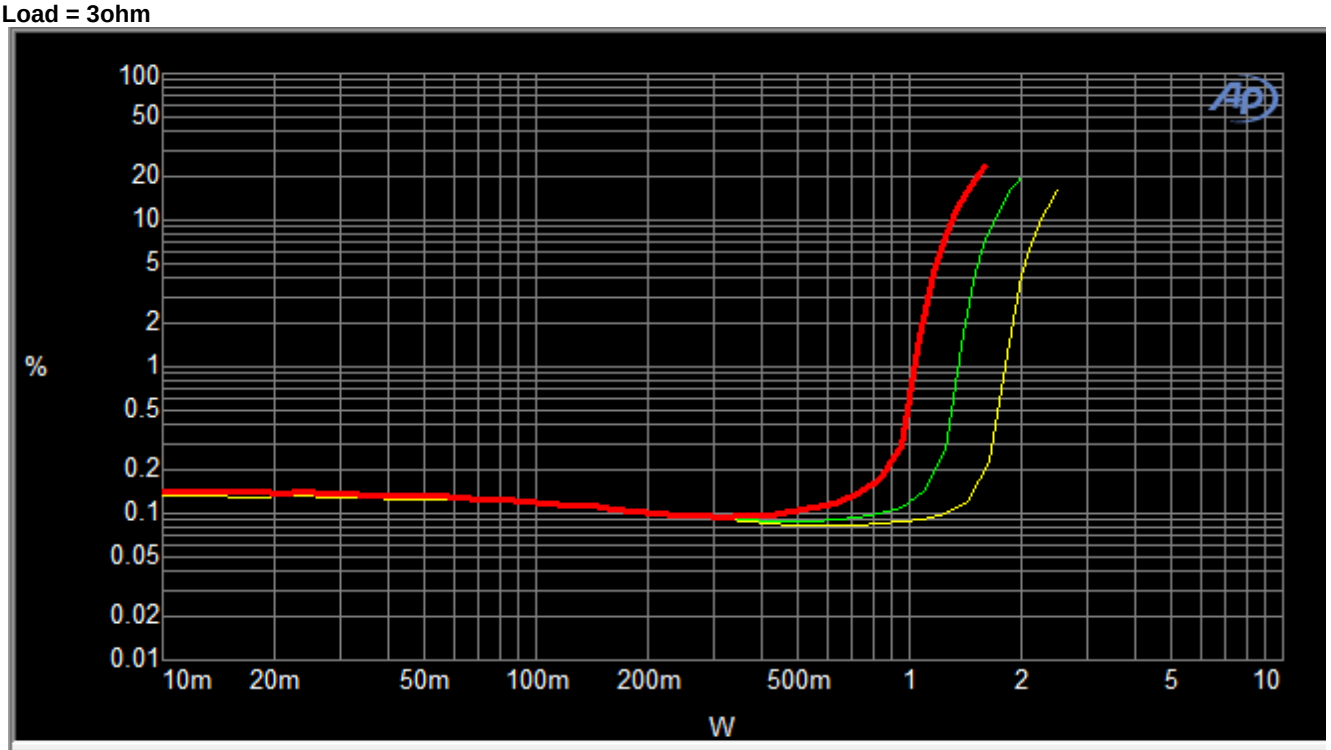



**Output Power vs THD+N**



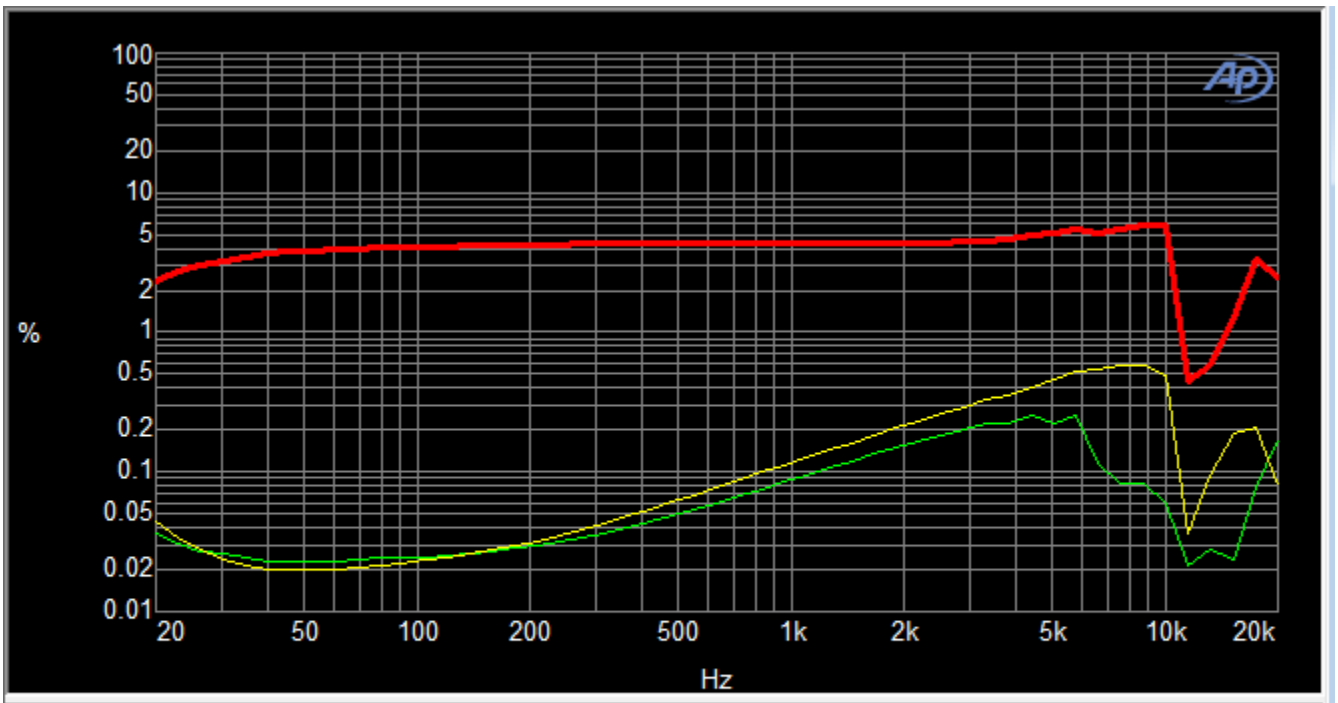

**$f_{IN}$ vs THD+N**

**Load = 3ohm**




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Green | Solid | 1 | Analyzer.THD+N I | Left | 3.7V |
| 2 | 1 | Yellow | Solid | 1 | Analyzer.THD+N F | Left | 4.2V |
| 3 | 1 | Red | Solid | 1 | Analyzer.THD+N I | Left | 3.3V |

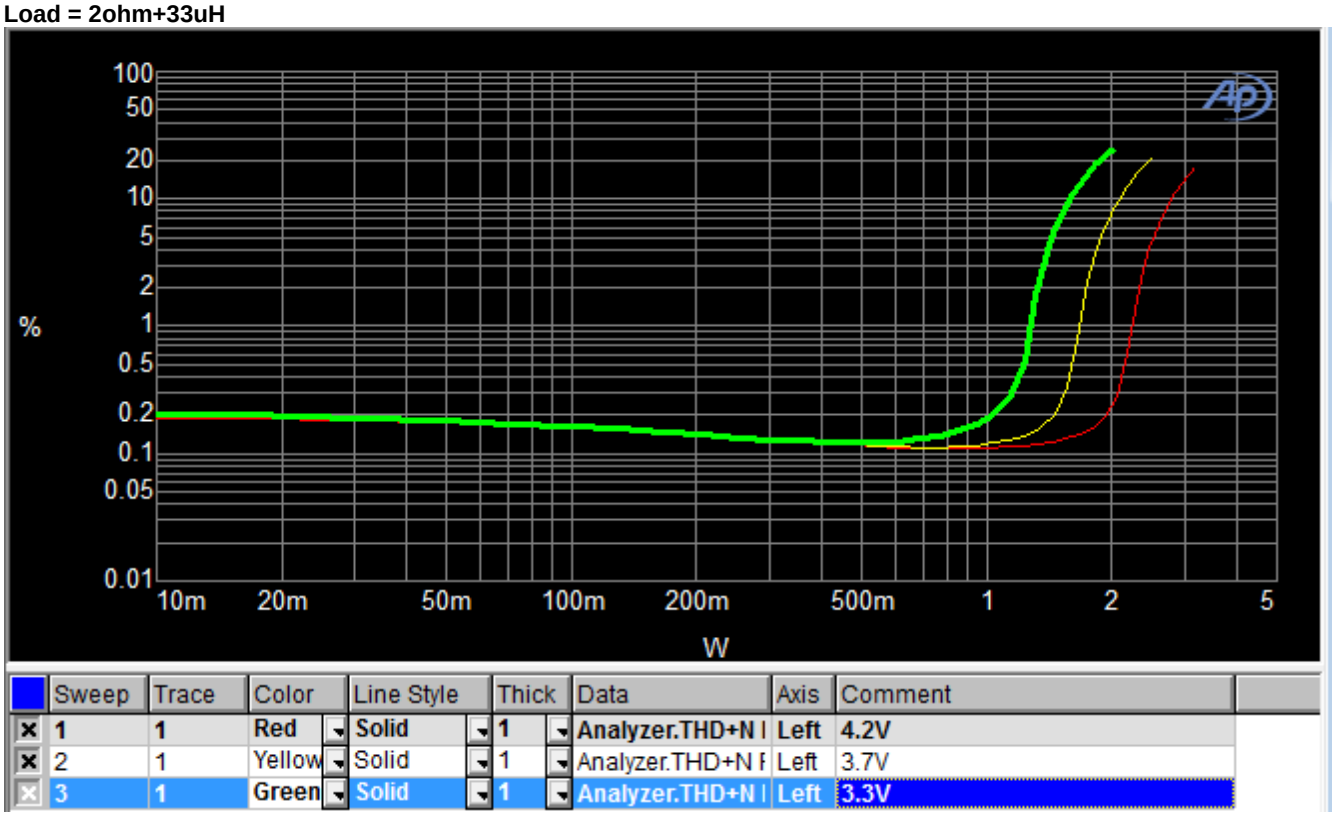
**Output Power vs THD+N**




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Green | Solid | 1 | Analyzer.THD+N I | Left | 3.7V,0.5W |
| 2 | 1 | Yellow | Solid | 1 | Analyzer.THD+N F | Left | 3.7V,1W |
| 3 | 1 | Red | Solid | 1 | Analyzer.THD+N I | Left | 3.7V,1.5W |

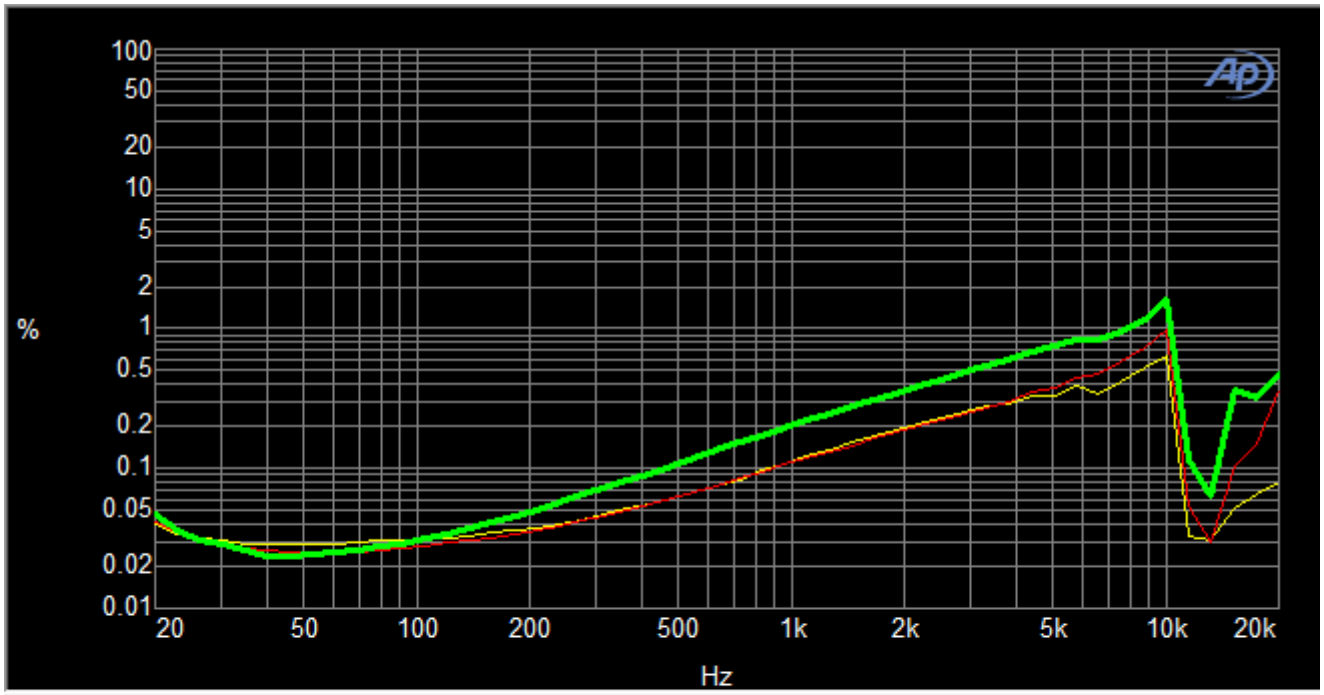
**$f_{IN}$ vs THD+N**

**Load = 2ohm+33uH**




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Red | Solid | 1 | Analyzer.THD+N I | Left | 4.2V |
| 2 | 1 | Yellow | Solid | 1 | Analyzer.THD+N F | Left | 3.7V |
| 3 | 1 | Green | Solid | 1 | Analyzer.THD+N I | Left | 3.3V |

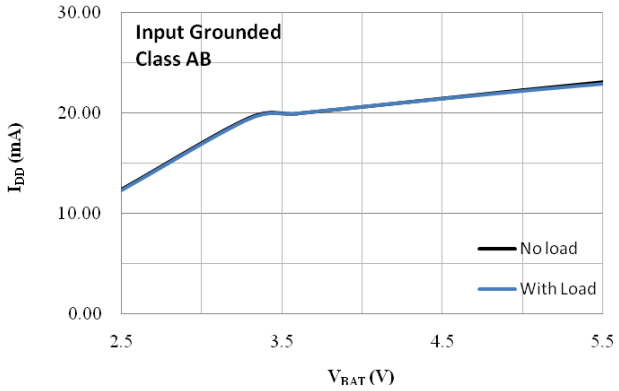
**Output Power vs THD+N**



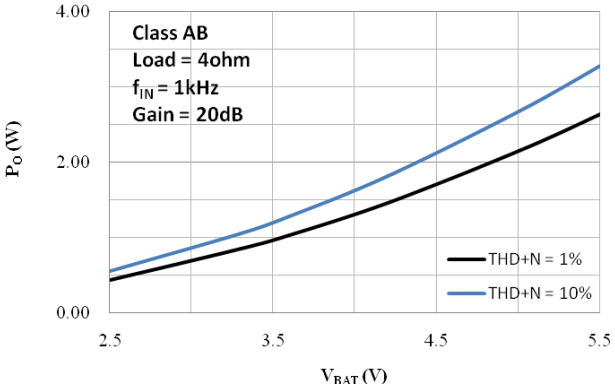

| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Yellow | Solid | 1 | Analyzer.THD+N I | Left | 3.7V,0.5W |
| 2 | 1 | Red | Solid | 1 | Analyzer.THD+N F | Left | 3.7V,1W |
| 3 | 1 | Green | Solid | 1 | Analyzer.THD+N I | Left | 3.7V,1.5W |

**$f_{IN}$ vs THD+N**

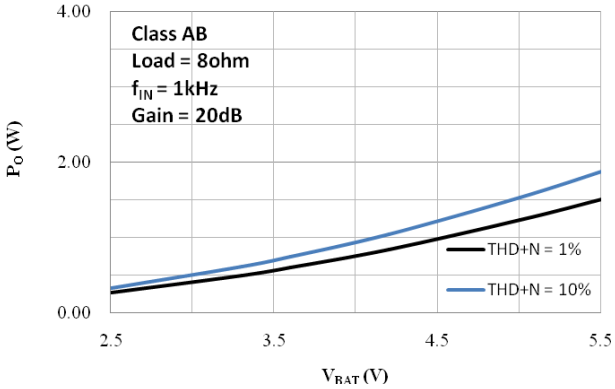
## $V_{BAT}$ vs $I_{DD}$



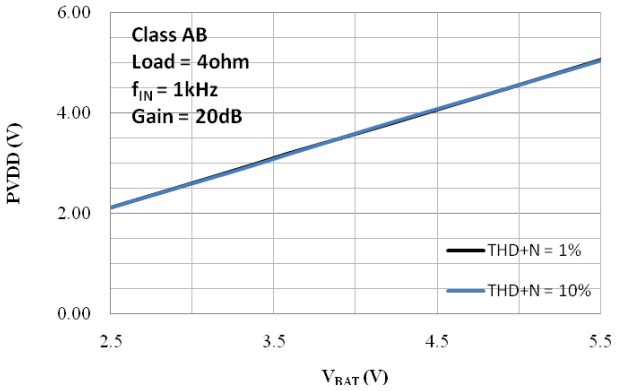

## $V_{BAT}$ vs $P_O$



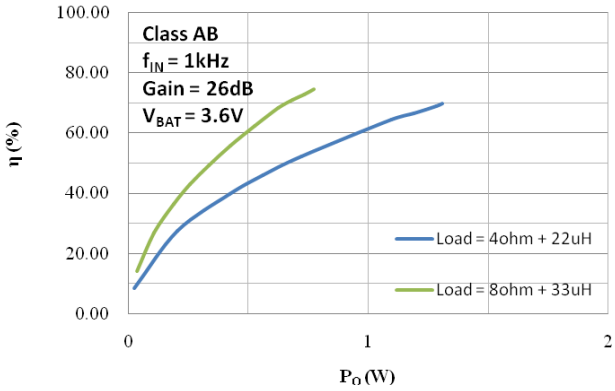

## $V_{BAT}$ vs $P_O$




## $V_{BAT}$ vs PVDD




## $P_O$ vs η



## ■ APPLICATION INFORMATION

The HT5169 is a flexible and easy-to-use mono class-D speaker amplifier with an digital input serial audio port. The HT5169 supports a variety of audio clock between 8kHz to 192kHz sample rate. The integrated boost conveter allows a higher output power with battery supply.

HT5169 是一颗简单易用且灵活的数字输入 D 类音频功放，其支持 8k~192kHz 的采样频率。其内置的升压电路，可为锂电池输入应用条件下提供更高的输出功率。

### 1 Power Supplies

Only two power supplies are required for the HT5169. They are a 3.3-V power supply, called DVDD and AVDD for the small signal digital and analog and a higher voltage power supply, and called VBAT for the input power supply of boost converter.

HT5169 仅需要两种电源供电，即在 DVDD（数字电源）和 AVDD（模拟电源）端加 3.3V，以及升压电路输入端 VBAT。

### 2 Speaker Amplifier Audio Signal Path

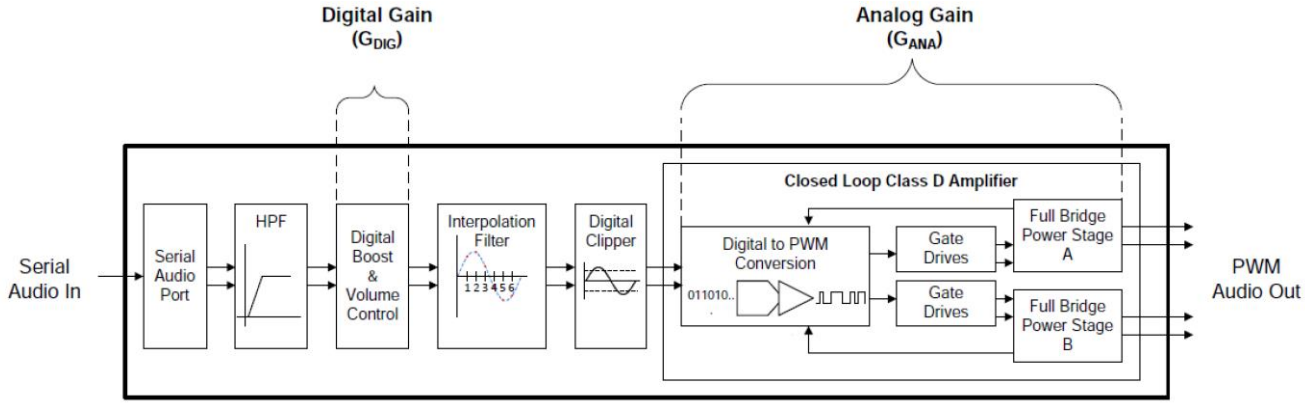



Figure 1 Speaker Amplifier Audio Signal Path

#### 2.1 Serial Audio Port

The serial audio port receives audio in either I²S, Left Justified, Right Justified or TDM formats, up to 32-bit word length. Default setting is I²S and 32-bit word length. The supported clock rates and ratios are detailed below.

HT5169 的数字音频串行输入接口支持 I²S、左对齐、右对齐、TDM 等数据格式，最高支持 32 bit 字长（SCLK = 32×2 fs）。默认设置为 I²S、32 bit 字长。支持的相关时钟速率和比例如下表。

Table1 Supported SCLK rates for TDM

| Maximum Sample Rate fs (kHz) | SCLK Rate (xfs) |
|---|---|
| 8-48kHz | 128, 256, 512 |
| 96kHz | 128, 256 |
| 192kHz | 128 |

Table2 Supported SCLK rates for IIS/LJ/RJ

| Sample Rate fs (kHz) | MCLK rate (× fs) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 128 | 192 | 256 | 384 | 512 | 768 | 1024 | 1152 |
| | SCLK rate (× fs) | | | | | | | |
| 8 | N/S | N/S | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | N/S | N/S |
| 12 | N/S | N/S | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | N/S | N/S |
| 16 | N/S | N/S | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | N/S |
| 24 | N/S | N/S | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | N/S |
| 32 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 |
| 38 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | N/S |
| 44.1 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | N/S |
| 48 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | N/S |
| 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | N/S | N/S |
| 88.2 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | N/S | N/S | N/S | N/S |
| 96 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | N/S | N/S | N/S | N/S |
| 128 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | 32, 48, 64 | N/S | N/S | N/S | N/S |
| 176.4 | 32, 48, 64 | 32, 48, 64 | N/S | N/S | N/S | N/S | N/S | N/S |
| 192 | 32, 48, 64 | 32, 48, 64 | N/S | N/S | N/S | N/S | N/S | N/S |

2.1.1 I²S

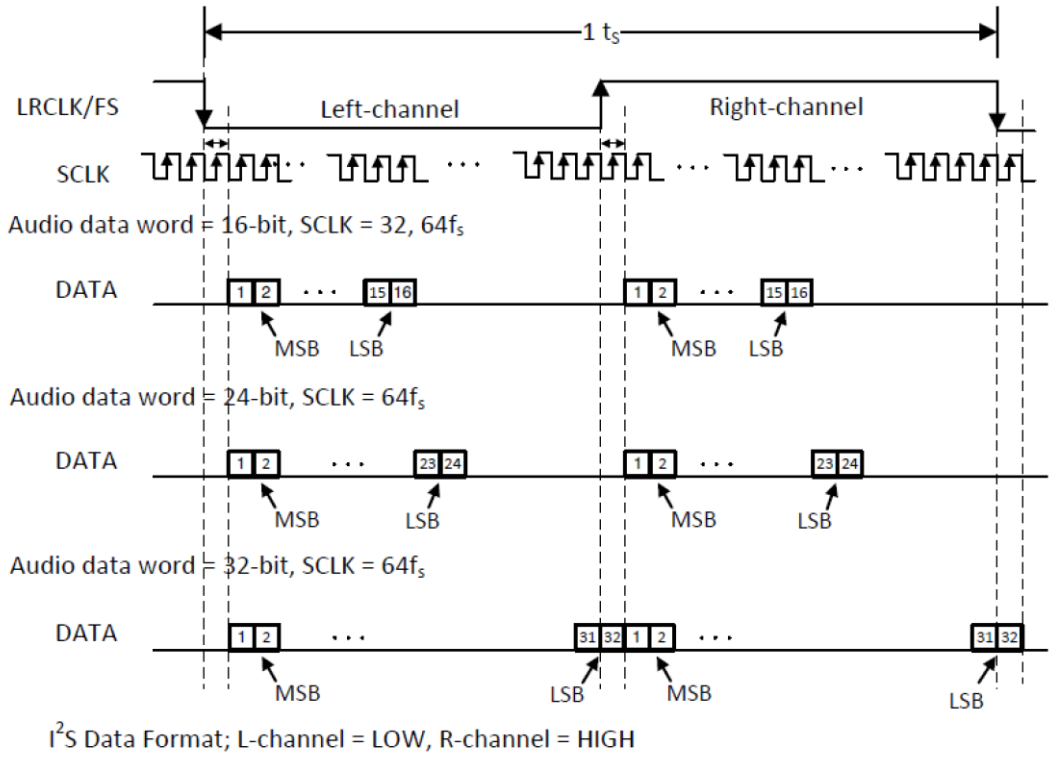



Figure 2 IIS Audio Data Format Timing

2.1.2 Left-Justified

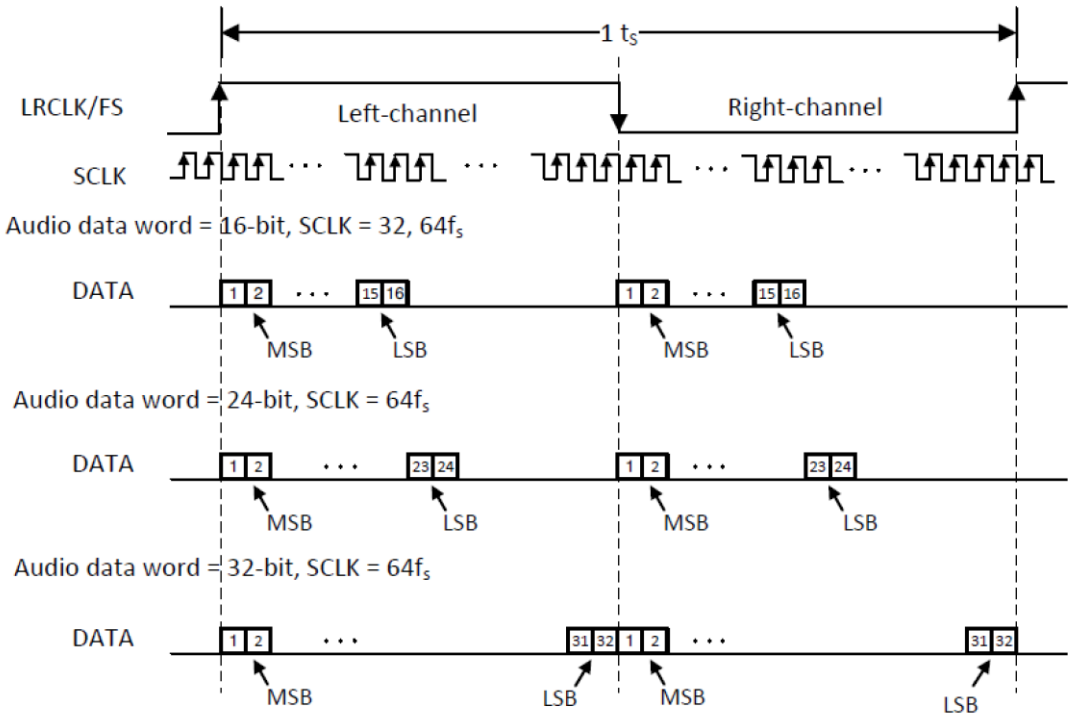



Figure 3 Left-Justified Audio Data Format Timing

2.1.3 Right-Justified

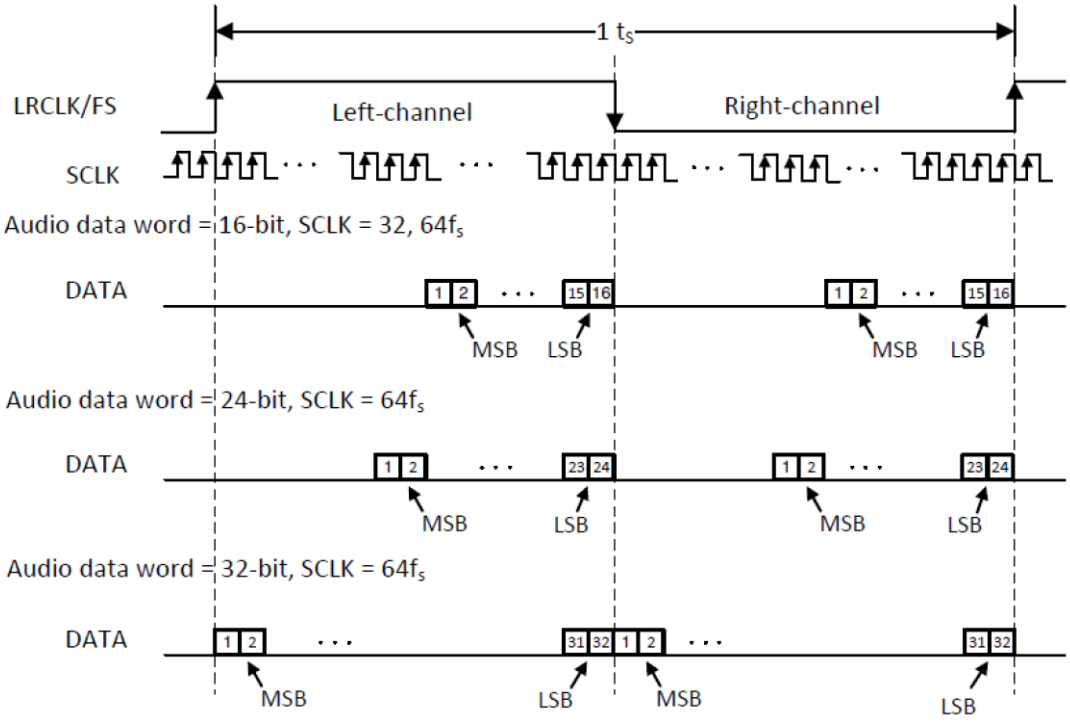



Figure 4 Right-Justified Audio Data Format Timing

2.1.4 TDM

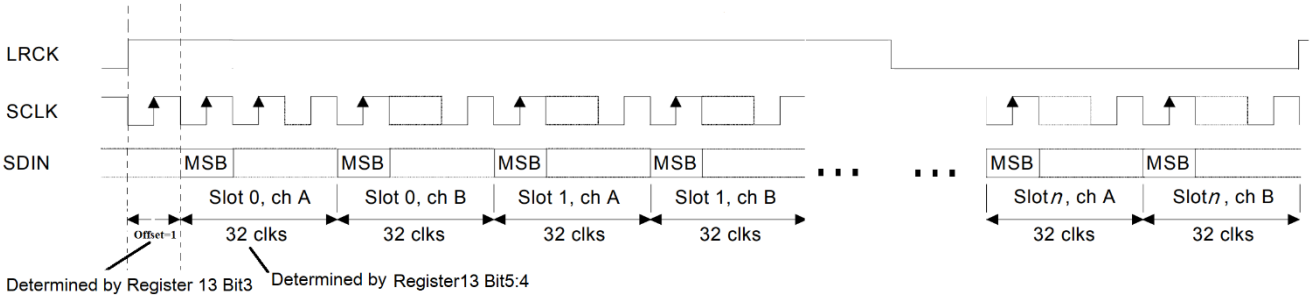



Figure 5 TDM Audio Data Format Timing

## 2.2 DC Blocking Filter

Excessive DC content in the audio signal can damage loudspeakers and even small amounts of DC offset in the signal path cause audible artifacts when muting and unmuting the speaker amplifier. For these reasons, the amplifier employs a DC blocking methods for the speaker amplifier which is a high-pass filter provided at the front of the data path to remove any DC from incoming audio data before it is presented to the audio path. In Hardware Control mode, the DC blocking filter is active and cannot be disabled. In software Control mode, the filter can be bypassed by writing a 0 to bit 7 of register 0x14.

音频信号持续的直流成分，可能损坏喇叭，或者产生输出直流偏置进而在静音/解除静音时产生噪声。因此，HT5169 具有隔直流的方式，即在数据通道前端设置高通滤波器，以在数据输入端去除直流成分。在硬件工作模式，该滤波器不能关闭；在软件控制模式，该滤波器可关闭（0x14 寄存器的 bit7）。

## 2.3 Digital Boost and Volume Control

Following the high-pass filter, a digital boost block is included to provide additional digital gain if required for a given application as well as to set an appropriate clipping point for a given GAIN configuration. The digital boost block defaults to +0dB and is changeable through bit [1:0] of register 14. In most use cases, the digital boost block will remain unchanged, as the volume control offers sufficient digital gain for most applications. The HT5169's digital volume control operates from Mute to 24 dB, in steps of 0.5 dB. The equation below illustrates how to set the 8-bit volume control register at address 0x15/0x16:

DVC [Hex Value] = 0xCF + (DVC [dB] / 0.5 [dB])

Transitions between volume settings will occur at a rate of 0.5 dB every 8 LRCK cycles to ensure no audible artifacts occur during volume changes. This volume fade feature can be disabled via Bit 4 of Register 0x14.

在高通滤波隔直后是数字增加模块，该模块可为数字信号提供一个附加的数字增益，以适应不同的应用。其默认设置是+0dB，可通过 0x14 寄存器的 bit[1:0]修改。在大多数情况下，其设置后不用修改。

HT5169 的数字音量控制可通过 0x15 和 0x16 寄存器设置 Mute~+24dB（每步 0.5dB）。下面是如何设置该寄存器的公式：

DVC [Hex Value] = 0xCF + (DVC [dB] / 0.5 [dB])

数字音量的变化速率为 0.5dB/8LRCK，以避免音量突变产生噪声。这种音量渐变的功能可通过 0x14 寄存器的 bit4 关闭。

### 2.4 Digital Clipper

A digital clipper is integrated in the oversampled domain to provide a component-free method to set the clip point of the speaker amplifier. Through the "Digital Clipper Level x" (at register address 0x10, 0x11, 0x12) controls in the I²C control port, the point at which the oversampled digital path clips can be set directly, which in turns sets the 10% THD+N operating point of the amplifier. This is useful for applications in which a single system is designed for use in several end applications that have different power rating specifications. Its place in the oversampled domain ensures that the digital clipper is acoustically appealing and reduces or eliminates tones which would otherwise foldback into the audio band during clipping events. Figure 6 shows a block diagram of the digital clipper.

HT5169 集成了数字限幅器，无需任何元器件、仅通过寄存器（0x10, 0x11, 0x12）配置即可设置功放输出的削顶幅度，即功放 10% THD+N 工作点。其在一种硬件设计适应多种不同功率等级的应用终端时特别有用。

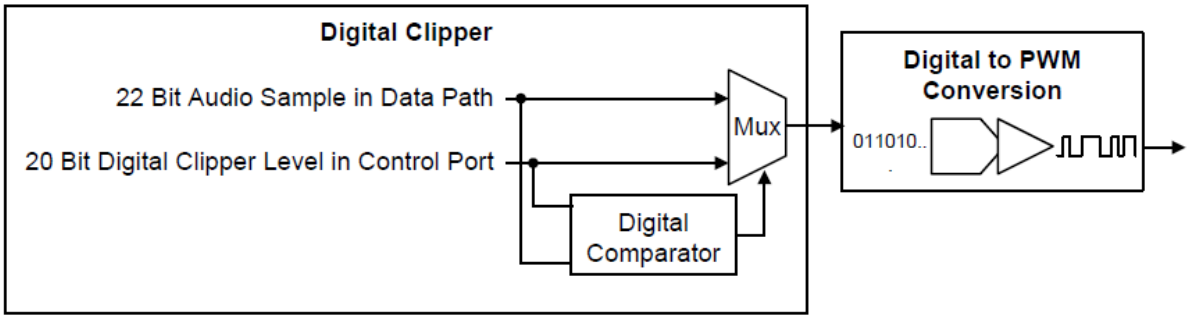



Figure 6 Digital Clipper Simplified Block Diagram

It is important to note that the actual signal developed across the speaker will be determined not only by the digital clipper, but also the analog gain of the amplifier. Depending on the analog gain settings and the PVDD level applied, clipping could occur as a result of the voltage swing that is determined by the gain being larger than the available PVDD supply rail.

需要了解的是，功放输出的最终幅度不止取决于该限幅器，还取决于当前设置的模拟增益和 PVDD 电压。

### 2.5 Closed-Loop Class-D Amplifier

Following the digital clipper, the interpolated audio data is next sent to the Closed-Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse width modulated (PWM) signals which are used to drive the outputs of the speaker amplifier. Feedback loops around the DPC ensure constant gain across supply voltages, reduce distortion, and increase immunity to power supply injected noise and distortion. The analog gain is also applied in the Class-D amplifier section of the device.

The switching rate of the amplifier is around 410 kHz by default, and can be changed through bit 0 of register 0x19.

数字信号经过数字限幅器后，进入了闭环 D 类功放。D 类功放的第一级是数字转 PWM 模块（DPC），PWM 信号则被用来驱动功放输出级。DPC 的反馈环可保证恒定的增益，降低失真，提高对电源噪声的免疫力。该 D 类功放的模拟增益（GAIN_A）可通过寄存器修改。

D 类功放的默认开关频率在 410kHz 附近，可通过寄存器 0x19 的 bit0 修改。

## 3 Speaker Amplifier Protection Suite

The speaker amplifier in the HT5169 includes a robust suite of error handling and protection features. It is protected against Over-Current, Over-Voltage, Over-Temperature, and Clock Errors. The status of some errors is reported via the FAULT pin or/and the appropriate error status register in the I²C Control Port. Table3 details the types of errors protected by the HT5169 Protection Suite and how each are handled.

HT5169 具有多种保护功能，包括过流、过压、过温、时钟错误等保护。某些故障将通过\FAULT 引脚和/或寄存器错误标志位反应。下表对这些故障和保护进行了详细说明。

Table3 Protection Suite Error Handling Summary

| ERROR | CAUSE | Reported Method | The device resumes normal operation |
|---|---|---|---|
| Overvoltage Error (OVE) | PVDD level rises above that specified by $OVE_{RTH}$ | None | Immediately after PVDD level returning below $OVE_{FTH}$ |
| Clock Error (CLKE) | One or more of the following errors has occurred:<br>1. Non-supported MCLK to LRCK and/or SCLK to LRCK Ratio;<br>2. Non-supported MCLK or LRCK rate<br>3. MCLK, SCLK, or LRCK has stopped | \FAULT and Register | Immediately after Clocks returning to valid state |
| Overcurrent Error (OCE) | Speaker Amplifier output current has increased above the level specified by $OCE_{TH}$ | None | After a period of $T_{fault}$ |
| Overtemperature Error (OTE) | The temperature of the die has increased above the level specified by the $OTE_{TH}$ | None | After a period of $T_{fault}$ |

### 3.1 \FAULT pin

In both hardware and software Control mode, the \FAULT pin of the HT5169 serves as a fault indicator to notify the system that a fault of clock error has occurred with the device by being actively pulled LOW. This pin is an open-drain output pin and, unless one is provided internal to the receiver, requires an external pullup to set the net to a known value. The behavior of this pin varies based upon the type of error which has occurred.

在硬件工作模式和软件控制模式，HT5169 的\FAULT 脚作为故障显示，当芯片发生时钟错误的故障时，该引脚拉低。该引脚是开漏结构的输出脚，需要在外部通过电阻上拉至固定电平，或连接至主控 I/O。

### 3.2 Over-Current Protection

The HT5169 features over-current conditions against the output stage short-circuit conditions. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is triggered. The device will automatically attempt to resume after Tfault. If the over-current condition is still not cleared, the device will again go into protection.

HT5169 输出级短路时，发生了过流，此时芯片进入保护状态，功放输出切换到高阻状态。经过 $t_{FAULT}$ 时间后，芯片将自动尝试恢复，若过流状态已消失，芯片恢复；若过流状态仍在，芯片再次进入保护状态。

### 3.3 Over-temperature Protection

Over-temperature protection on the HT5169 device prevents damage to the device when the internal die temperature exceeds 150°C. This triggering point has a ±15°C tolerance from device to device. Once the die temperature exceeds the thermal triggering point, the device is switched to the shutdown state and the outputs are disabled. The device will automatically attempt to resume after $T_{fault}$. If the over-temperature condition is still not cleared, the device will again go into protection.

过温保护在芯片内部结温达到 150℃时发生，以防止芯片损坏，此时芯片进入关断状态。经过 $t_{FAULT}$ 时间后，芯片将自动尝试恢复，若过温状态已消失，芯片恢复；若过温状态仍在，芯片再次进入保护状态。

### 3.4 Over-voltage Protection

The HT5169 device monitors the voltage on PVDD voltage threshold. When the voltage on PVDD pin exceeds the over-voltage threshold, the OVP circuit puts the device into shutdown mode. The device recovers automatically once the over-voltage condition has been removed.

当 PVDD 电压高于过压保护点（$OVE_{RTH}$）时，芯片进入保护状态，芯片关闭。当 PVDD 低于过压保护点（$OVE_{FTH}$）后，芯片立即自动恢复。

### 3.5 Clock error detection

When any clock of MCLK, SCLK, LRCK halt or shifted to a non-supported speed, the device reports Clock Error in bit [1:0] of Register 0x17 and \Fault pin. The device recovers automatically once the clock-error condition has been removed.

当 MCLK、SCLK、LRCK 停止或为不支持的速率时，芯片进入保护状态，\FAULT 脚拉低，寄存器 0x17 的 bit[1:0]标志位进行相应显示。当故障撤销时，芯片立即自动恢复，\FAULT 恢复高，寄存器标志位恢复。

## 4 Device Functional Modes

### 4.1 Software Control and Hardware Control

The HT5169 device can be configured via an I²C communication port which is software control mode. Once all powers (VBAT, AVDD, DVDD) are brought up and stable, the device is ready for software control. Before the device is configured into operation (that is bring \SD pin to high, or write Bit “SD” into 1), configure the device via I²C in the manner required by the use case, e.g., bit “Format”.

For systems which do not require the added flexibility of the I²C control port or do not have an I²C host controller, the HT5169 can be used directly in Hardware Control Mode with default configurations. The only external I/O that can be controlled in Hardware Control Mode is the \SD pin.

HT5169 可以通过 I²C 通讯端口进行配置，即软件控制模式。当 VBAT、AVDD、DVDD 已稳定，芯片的软件控制模式即已准备就绪。在芯片进入工作状态（即将\SD 脚拉高，或将 Bit “SD” 写 1）前，需要通过 I²C 将芯片配置成需要的状态（如 bit “Format”等）。

对于不需要灵活的配置，或没有 I²C 主机的应用，HT5169 可工作在硬件模式，此时芯片工作在默认配置，外部唯一可控制的端口即为\SD。

### 4.2 Speaker Amplifier Shut Down (\SD pin)

The \SD pin is provided to place the speaker amplifier into shutdown. Driving this pin LOW will place the device into shutdown, while pulling it HIGH will bring the device into operation. The shutdown mode is the lowest power consumption mode that the device can be placed in while the power supplies are up.

However, when \SD pin is pulled low, the software control mode is ready, the device is still capable of being configured through I²C port. If the \SD pin is pulled low, and bit SD is written into 1, the device is in operation mode. See as the following table.

\SD 脚拉低时，芯片进入关断模式；\SD 拉高时，芯片进入工作状态。在关断模式下，芯片进入低功耗状态。

需要注意的是，\SD 拉低时，芯片的软件控制模式仍处于准备就绪状态，芯片仍可通过 I²C 控制，此时若将 Bit SD 写 1，芯片仍可进入工作状态。如下表。

Table4 \SD pin and Bit SD

| \SD pin | Bit SD | Mode |
|---|---|---|
| LOW | 1 | Normal operation |
| LOW | 0 | Shutdown mode |
| High | 0 | Normal operation |
| High | 1 | Normal operation |

### 4.3 Operating Modes

The HT5169 device can be used with 3 different operation modes, can be configured by Register 0x19: Class D mode in ACF-off mode with boost converter on, Class D mode in ACF-on mode with boost converter on, Class AB mode in ACF-off mode with boost converter off.

HT5169 可通过寄存器 0x19 设置不同的工作模式：

D 类模式, ACF-off, 升压开启；

D 类模式, ACF-on, 升压开启；

AB 类模式, ACF-off, 升压关闭；

#### 4.3.1 ACF-on Mode

In ACF-ON modes, HT5169 attenuates system gain to an appropriate value when an excessive input is applied, so as not to cause the clipping at the differential signal output. In this way, the output audio signal is controlled in order to obtain a maximum output level without distortion. And HT5169 also follows to the clips of the output waveform due to the decrease in the power-supply voltage.

The Attack time of ACF Function is a time interval until system gain falls to target attenuation gain -3dB when a big enough signal input. And, the Release Time is a time from target attenuation gain to not working of ACF. The maximum attenuation gain is 16dB.

在 ACF-ON 模式下，当电路检测到输入信号幅度过大而产生输出削顶时，HT5169 通过自动调整系统增益，控制输出达到一种最大限度的无削顶失真功率水平，由此改善了音质效果。

此外，当 PVDD 下降时，HT5169 也能自动衰减输出增益，实现与 PVDD 下降值相匹配的最大限度无削顶输出水平。

ACF ON 模式下的启动时间（Attack time）指在突然输入足够大信号，系统减小到目标增益 -3dB 的时间；释放时间（Release time）指产生削顶的输入条件消失，增益退出衰减状态的时间。HT5169 的最大衰减增益为 16dB。

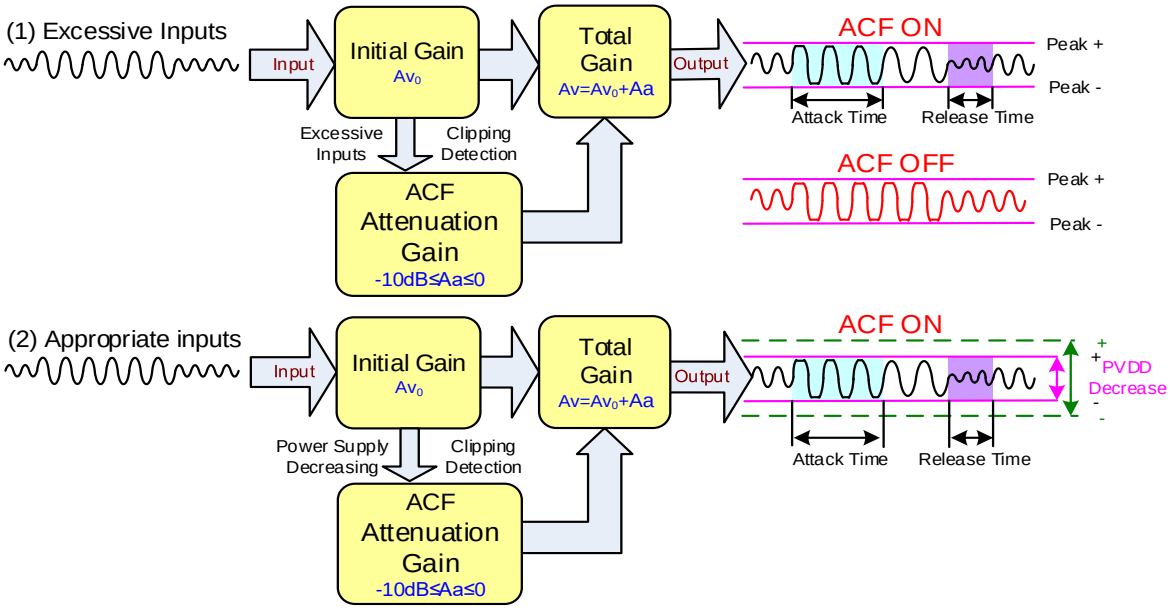



Figure 7 the ACF Function Operation Outline

Table5 Attack time and Release time

| ACF mode | Attack time | Release time |
|---|---|---|
| ACF-ON | 50ms | 64ms |

#### 4.3.2 ACF-off Mode

In ACF-Off mode, ACF function is disenabled. HT5169 will not detect output clipping and the system gain is kept to be Av=Av0. The audio quality would worsen due to clipping distortion.

在 ACF-Off 模式下，ACF 功能被关闭，HT5169 不对输出削顶条件作检测，也不对系统增益作自动调整操作，系统增益保持为 Av=Av0 恒定不变。HT5169 可能因输出存在破音失真而音质变坏。

#### 4.3.3 Class AB Mode

HT5169 works as Class AB audio Amplifier when EMI is highly concerned (such as FM applications). In this mode, ACF function is off, and the boost converter is disenabled.

当 EMI 要求严格（如 FM 场合），HT5169 可以工作在 AB 类模式，此时 ACF-off, 升压关闭。

### 4.4 BOOST Converter

The HT5169 integrates a boost convter that converts the input power VBAT into a higher voltage PVDD which serves as the power supply of audio power amplifier.

HT5169 内置了升压电路，将 VBAT 电压升至 PVDD，供功放供电。

#### 4.4.1 Setting Output Voltage

The output voltage PVDD is set by a resistive voltage divider from the output voltage to FB terminal, which is shown below. The output voltage can be calculated by PVDD = 1.24*(Rd1+Rd2)/Rd2. Some typical output voltages can be got by following settings.

Boost 升压模块的输出电压 PVDD 可由外部配置，如下图所示，PVDD = 1.24*(Rd1+Rd2)/Rd2。建议取值如下表，并可根据实际应用进行微调。

。

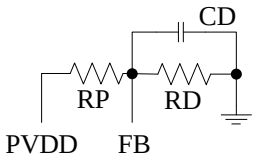



Figure 8 FB Terminal Configuration

Table6 Output Voltage Setting

| PVDD | RP | RD | CD |
|---|---|---|---|
| 5.0V | 510K | 165K | 3.3nF |
| 6.5V | 510K | 120K | 3.3nF |
| 7.0V | 510K | 110K | 3.3nF |
| 7.5V | 510k | 100k | 3.3nF |

#### 4.4.2 LX Terminal

It is strongly recommended to place an RC circuit from the terminal of LX to Ground, shown as following, so that the ripple current of Boost Converter can be decreased. Meanwhile, the total consumption current of the system will be larger so that the efficiency of the system will be lower. Specifications in this file is measured under the condition with RC.

Notes: RC should be placed as closely to LX pin as possible.

在输出 PVDD 较大、使用功率较大、音乐波动较大的情况下，建议在 LX 端加入 RC，如图 2，能起到稳定 DCDC 的作用。引入此 RC，将增加板级的静态电流、并降低系统的效率，说明书中的相关数据均是在加入此 RC 后测得。

注意: RC 应尽可能靠近 LX 引脚放置。

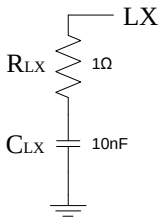



Figure 9 LX Terminal Configuration

#### 4.4.3 Capacitor Selection

The input and output capacitor ($C_{IN}$ and $C_{OUT}$) is required to maintain the DC voltage. Low ESR capacitors are preferred to reduce the output voltage ripple. 1uF//10uF//220uF (paralleled) is highly recommended to be placed in both input and output terminal as closely to the pin as possible. If possible, 470uF is better than 220uF.

由于输入电压 VBAT 经 BOOST 升压后的 PVDD 直接供电给音频功放，而音频功放在工作时对电源本身具有较大扰动，这时，电源端的滤波就非常重要。

我们建议，在 VBAT 和 PVDD 端至少放置一组 1uF 和 10uF 接地电容，用于吸收纹波和稳定电压，并尽可能靠近芯片引脚。另外，VBAT 和 PVDD 端需各放置一个不小于 220uF 的储能电容，如果可能，放置 470uF 电容。这些电容应以最短的路径连接至安静可靠的地，以有效滤波。

#### 4.4.4 Inductor Selection

The inductor is selected based on different conditions. Normally, L≥2.2uH, DCR<1ohm, and do make sure that $I_{SAT}$ is higher than the maximum peak current of input power supply..

为保证芯片的正常工作，建议使用 L≥4.7uH, DCR<1ohm, ISAT ≥ 2.5 A。在输出 PVDD 较大、使用功率较大、音乐波动较大的情况下，应适当选择 L 较大的电感。

#### 4.4.5 Schottky Diode Selection

$V_{RRM}$ > 12V, $V_{FM}$＜0.5V, and do make sure that $I_F$ is higher than the maximum current of output power supply.

为保证芯片的正常工作，建议使用 $V_{RRM}$ > 12V, $V_{FM}$＜0.5V, $I_F$≥1.5 A 的肖特基二极管。在输出 PVDD 较大、使用功率较大、音乐波动较大的情况下，应适当选择 $I_F$ 较大的肖特基二极管。

#### 4.4.6 Layout Consideration

The power traces, consisting of the GND, LX, VBAT and PVDD trace should be kept short, direct, wide, and as closely to the pin as possible. The switching node LX should be paid more attention for EMI and reliability consideration.

Place $C_{IN}$ and $C_{OUT}$ near VBAT and PVDD as closely as possible to maintain voltage steady, and filter out the pulsing current.

The resistive divider Rp and Rd should be connected to pin directly as closely as possible. FB is a sensitive node. Please keep it away from switching node, LX.

The GND of the IC, $C_{IN}$ and $C_{OUT}$ should be connected close together directly to ground plane

电源线（VBAT, PVDD，包括电源地回路），LX 线，应尽可能使用短、粗、无弯折的引线连接；应特别注意 LX 端引线，其开关频率会影响 EMI；

VBAT 和 PVDD 端 $C_{IN}$ 应尽可能靠近芯片引脚，以保证电压的稳定；

分压反馈电阻 Rp 和 Rd 应尽量靠近 FB，FB 引线应尽量远离干扰源，如 LX 端所连的电感、二极管等；

IC 的地，应尽可能以最短的路径和星形结构连接至稳定可靠的地。

### 4.5 I2C Control Port

#### 4.5.1 I²C Device Address

Each device on the I²C bus has a unique address that allows it to appropriately transmit and receive data to and from the I²C master controller. As part of the I²C protocol, the I²C master broadcast an 8-bit word on the bus that contains a 7-bit device address in the upper 7 bits and a read or write bit for the LSB. The HT5169 has a configurable I²C address. The ADR[1:0] can be used to set the device address of the HT5169. The I²C device address is configured as “11011xx [R/W]”, where “xx” corresponds to the state of the ADR[1:0] pin at first power up sequence of the device. [R/W] represents 1 when writing, [R/W] represents 0 when reading.

每个器件在 I²C 总线上具有一个独一无二的器件地址，以便正确的将数据传输至 I²C 主机及从 I²C 主机接收数据。作为 I²C 协议的一部分，I²C 主机在总线上广播一个 8 位字节，该字节包含高 7 位的 7 位设备地址和 LSB 的读或写位。HT5169 通过引脚 ADR[1:0]可设置 I²C 地址。I²C 地址即为 11011xx [R/W]，其中“xx”表示上电时引脚 ADR[1:0]的状态，当进行读操作时[R/W]代表 0，当进行写操作时[R/W]代表 1。

Table7 I²C Address Configuration

| ADR[1:0] | IIC Address for Reading | IIC Address for Writing |
|---|---|---|
| LL | 0xD8 | 0xD9 |
| LH | 0xDA | 0xDB |
| HL | 0xDC | 0xDD |
| HH | 0xDE | 0xDF |

### 4.5.2 General Operation of the I²C Control Port

The HT5169 device has a bidirectional I²C interface that is compatible with the Inter IC (I²C) bus protocol and supports both 100-kHz and 400-kHz data transfer rates. This is a slave-only device that does not support a multi-master bus environment or wait-state insertion.

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bi-directional bus using a wired-AND connection.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus.

HT5169 I²C 接口支持双向传输，该接口与 I²C 总线协议兼容，并支持 100 kHz 和 400 kHz 数据传输速率。这是一个从设备，不支持多主机的总线环境，及等待状态下的插入。

I²C 总线具有两个信号，SDA（数据）和 SCL（时钟），在系统中的器件之间使用串行数据传输进行通信。地址和数据的 8 位字节首先传输最高有效位（MSB）。此外，总线上传输的每个字节由接收设备用确认位（ACK）进行确认。每个传输操作从主设备驱动总线上的启动条件开始，并以主设备驱动总线上的停止条件结束。当时钟处于逻辑高电平时，总线使用数据终端（SDA）上的转换来指示启动和停止条件。SDA 上的高到低转换表示开始，低到高转换表示停止。正常的数据位转换必须在时钟为低时发生。

主机生成 7 位从机地址和读/写（R/W）位，以打开与另一个设备的通信，然后等待确认条件。在应答时钟周期内，设备保持 SDA 低，以指示确认。当发生这种情况时，主机发送序列的下一个字节。每个设备有唯一的 7 位从机地址加上 R/W 位（1 字节）。所有兼容设备通过并联的总线共享信息。

SDA 和 SCL 需通过外部上拉电阻截至逻辑高电平。

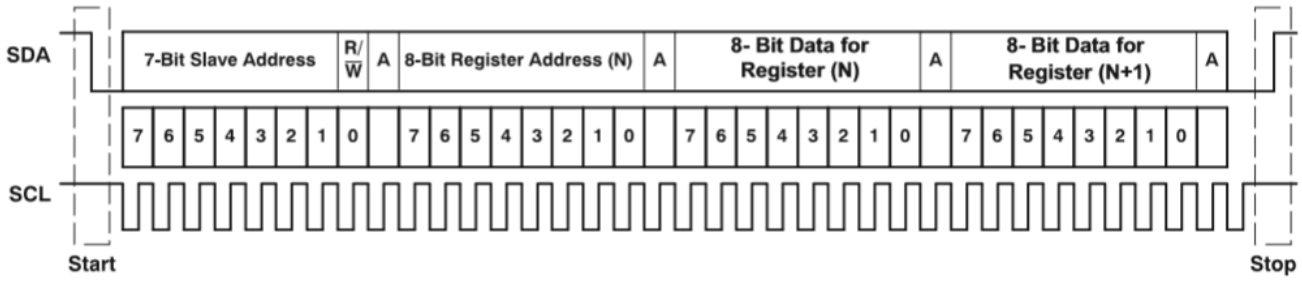



Figure 10 Typical I²C Sequence

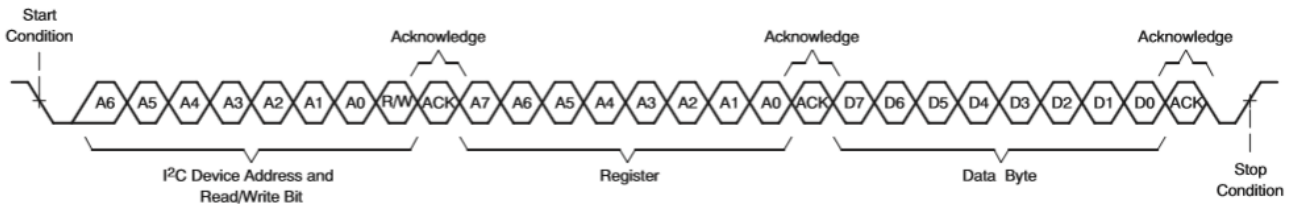



Figure 11 Single-Byte Write Transfer

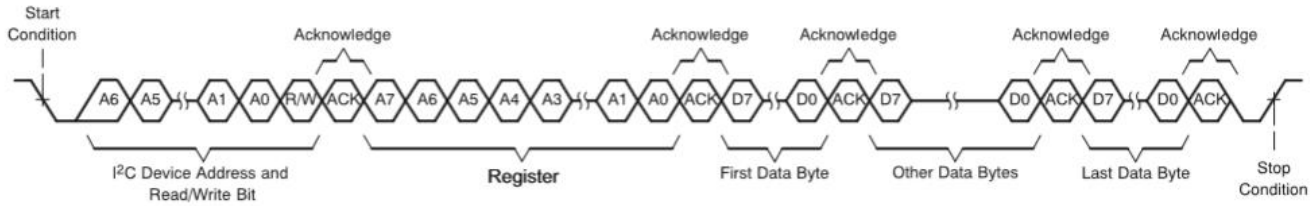


Figure 12 Multiple-Byte Write Transfer

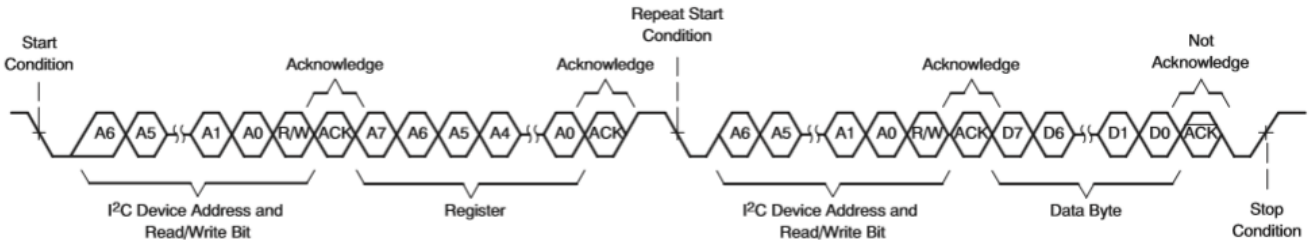



Figure 13 Single-Byte Read Transfer

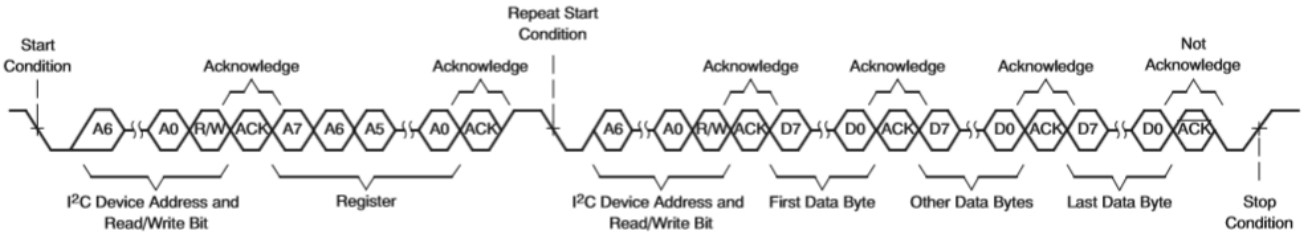



Figure 14 Multiple-Byte Read Transfer

## 5 Register Map

Table8 Register Map

| Register | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default Value |
|---|---|---|---|---|---|---|---|---|---|
| 0x10 | Digital Clipper Level DigClip[19:12] | | | | | | | | FFh |
| 0x11 | Digital Clipper Level DigClip[11:4] | | | | | | | | FFh |
| 0x12 | Digital Clipper Level DigClip[3:0] | | | | SLEEP | SD | MUTE_A | SPEED | F0h |
| 0x13 | Data Format | | Word_Length | | TDM_Offset | TDM_Slot | | | 00h |
| 0x14 | HPF Byps | Left_Mix | Right_Mix | Fade | MUTE_L | MUTE_R | Digital Boost | | 90h |
| 0x15 | Left channel volume control | | | | | | | | CFh |
| 0x16 | Right channel volume control | | | | | | | | CFh |
| 0x17 | ch_Shift | Fade_Mode | SCLK_DET_EN | CLK_DET_EN | Reserved | | CLK_Error | SCLK_Error | 33h |
| 0x18 | Reserved | Analog Gain | | | Reserved | | | | 02h |
| 0x19 | $f_{ClassD}$ | Operation Mode | | | Reserved | | | | 70h |

The register details are as follows. The blue fonts are the default settings when powering on.

寄存器详细信息如下。蓝色字体为上电时的默认设置状态。

### Register Address: 0x10 (default FFh)

| Bit | R/W | Label | Default | Description |
|---|---|---|---|---|
| 7:0 | R/W | DigClip[19:12] | FFh | The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level. |

### Register Address: 0x11 (default FFh)

| Bit | R/W | Label | Default | Description |
|---|---|---|---|---|
| 7:0 | R/W | DigClip[11:4] | FFh | The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level. |

The digital clipper level determined by DigClip[19:0] is the maximum output threshold level from DAC transferring to the analog Amplifier. The default value of the digital clipper level is the full scale of DAC output, and decreasing the value of DigClip[19:0] will decrease the digital clipper level as well.

### Register Address: 0x12 (default F0h)

| Bit | R/W | Label | Default | Description |
|---|---|---|---|---|
| 7:4 | R/W | DigClip[3:0] | 1111 | The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level. |
| 3 | R/W | SLEEP | 0 | 0: the device is not in the SLEEP mode;<br>1: the device is in the SLEEP mode.<br>In sleep mode, the analog Amp is muted, and the digital circuit works with lower current dissipation. |
| 2 | R/W | SD | 0 | 0: the device is shut down;<br>1: the device is not shut down;<br>Notice that if the device is truly shutdown also depends on the \SD pin, see **Speaker Amplifier Shut Down (\SD pin)** . |
| 1 | R/W | MUTE_A | 0 | 0: The analog Amp output is not muted<br>1: The analog Amp output is muted |
| 0 | R/W | SPEED | 0 | 0: Serial Audio Port will accept sample rates between 8k – 96kHz<br>1: Serial Audio Port will accept sample rates between 96kHz-192kHz |

### Register Address: 0x13 (default 00h)

| Bit | R/W | Label | Default | Description |
|---|---|---|---|---|
| 7:6 | R/W | Format | 00 | Control the Serial Audio Port data format<br>00: I²S<br>01 : Left justified<br>10: Rright justified<br>11: TDM |
| 5:4 | R/W | Word_Length | 00 | Control the Serial Audio Port sample word length<br>00: 32bits<br>01: 24 bits<br>10: 20bits<br>11: 16bits |
| 3 | R/W | TDM_Offset | 0 | Control the offset of TDM data in the audio frame. The offset is defined as the number of SCLK from starting (MSB) of audio frame to the starting of the desired audio sample, see Figure 5 TDM Audio Data Format.<br>0: offset = 0 SCLK<br>1: offset = 1 SCLK |
| 2:0 | R/W | TDM_Slot | 000 | Control the slot number of TDM data in the audio frame. The slot number is defined as Figure 5 TDM Audio Data Format.<br>000: Slot0_A + Slot0_B;<br>001: Slot1_A + Slot1_B;<br>…<br>111: Slot7_A + Slot7_B; |

### Register Address: 0x14 (default 90h)

| Bit | R/W | Label | Default | Description |
|---|---|---|---|---|
| 7 | R/W | HPF Byps | 1 | 0: The internal high-pass filter in the digital path is bypassed<br>1: The internal high-pass filter in the digital path is not bypassed |
| 6 | R/W | Left_Mix | 0 | 0: Left channel mixer is disabled<br>1: Left channel mixer is enabled, so that left = 1 / 2(left+right) |
| 5 | R/W | Right_Mix | 0 | 0: Right channel mixer is disabled<br>1: Right channel mixer is enabled, so that right = 1 / 2(left+right) |
| 4 | R/W | Fade | 1 | 0: Volume fading is disabled;<br>1: Volume fading is enabled |
| 3 | R/W | MUTE_L | 0 | MUTE the L channel digital output:<br>0: the left channel is not muted<br>1: the left channel is muted |
| 2 | R/W | MUTE_R | 0 | MUTE the R channel digital output:<br>0: the right channel is not muted<br>1: the right channel is muted |
| 1:0 | R/W | Dig Bst | 00 | Digital Boost setting<br>00: +0dB is added to the signal in the digital path<br>01: +6dB is added to the signal in the digital path<br>10: +12dB is added to the signal in the digital path<br>11: +18dB is added to the signal in the digital path |

### Register Address: 0x15 (Default CFh)

| Bit | R/W | Label | Default | Description |
|---|---|---|---|---|
| 7:0 | R/W | Vol_L | CFh | Left channel Volume control<br>1111,1111: +24dB;<br>1111,1110: 23.5dB<br>……Gain decreased by 0.5dB every step<br>1100,1111: 0dB<br>……Gain decreased by 0.5dB every step<br>0000,0111: -100dB<br>Any setting less than 0000,0111 places the channel in MUTE |

### Register Address: 0x16 (Default CFh)

| Bit | R/W | Label | Default | Description |
|---|---|---|---|---|
| 7:0 | R/W | Vol_R | CFh | Left channel Volume control<br>1111,1111: +24dB;<br>1111,1110: 23.5dB<br>……Gain decreased by 0.5dB every step<br>1100,1111: 0dB<br>……Gain decreased by 0.5dB every step<br>0000,0111: -100dB<br>Any setting less than 0000,0111 places the channel in MUTE |

### Register Address: 0x17 (default 33h)

| Bit | R/W | Label | Default | Description |
|---|---|---|---|---|
| 7 | R/W | ch_Shift | 0 | 0: The left and right channels are not shifted<br>1: The left and right channels are shifted |
| 6 | R/W | Fade_Mode | 0 | 0: The volume is fading by 0.5dB/8$T_{LRCK}$<br>1: The volume is fading by 0.5dB/$T_{LRCK}$ |
| 5 | R/W | SCLK_DET_EN | 1 | SCLK error detection, such as SCLK missing detection, SCLK range detection, SCLK/LRCK detection. If error detection is enabled, once any such error is detected, the relevant error flag will change to 1.<br>0: SCLK error detection is disabled;<br>1: SCLK error detection is enabled. |
| 4 | R/W | CLK_DET_EN | 1 | Audio serial port clock error detection, including SCLK, MCLK, LRCK. Once any error such as missing or wrong range of these clocks is detected, the relevant error flag will change to 1.<br>0: CLOCK error detection is disabled;<br>1: CLOCK error detection is enabled. |
| 3:2 | R | Reserved | 00 | Unused, make it always 00 |
| 1 | R | CLK_Error | 1 | Changes to 0 when Clock Error is detected;<br>back to 1 when Clock Error evacuated; |
| 0 | R | SCLK_Error | 1 | Changes to 0 when SCLK Error is detected;<br>back to 1 when SCLK Error evacuated; |

### Register Address: 0x18 (Default 02h)

| Bit | R/W | Label | Default | Description | |
|---|---|---|---|---|---|
| 7 | R | Reserved | 0 | Unused, make it always 0 | |
| 6:4 | R/W | A_GAIN | 000 | Set analog gain: (Not available yet) | |
| | | | | 000: Gain = 25.9dB (Class D); 19.3dB (Class AB) | 001: Gain = 22.7dB (Class D); 17.8dB (Class AB) |
| | | | | 010: Gain = 20.4dB (Class D); 16.5dB (Class AB) | 011: Gain = 18.6dB (Class D); 15.3dB (Class AB) |
| | | | | 100: Gain = 17.1dB (Class D); 14.3dB (Class AB) | 101: Gain = 15.8dB (Class D); 13.4dB (Class AB) |
| | | | | 110: Gain = 14.7dB (Class D); 12.6dB (Class AB) | 111: Gain = 13.7dB (Class D); 11.9dB (Class AB) |
| 3:0 | R | Reserved | 0010 | Unused, make it always 0010 | |

### Register Address: 0x19 (default 70h)

| Bit | R/W | Label | Default | Description |
|---|---|---|---|---|
| 7 | R/W | Class D Carrier clock frequency $f_{ClassD}$ | 0 | 0: 410kHz; 1: 480kHz<br>It is only changed when the device is brought from shutdown back into operation after this bit is changed. |
| 6:4 | R/W | Operation Mode | 111 | 111: Class D mode in ACF-off mode with boost converter enabled<br>100: Class D mode in ACF-on mode with boost converter enabled<br>010: Class AB mode in ACF-off mode with boost converter disabled |
| 3:0 | R | Reserved | 0000 | Unused, make it always 000 |

# 6 Typical Applications

## 6.1 Startup Procedures

1. Configure I/O pins (ADR[1:0]);
2. \SD pin = Low;
3. Bring up power supplies (it does not matter if VBAT, AVDD or DVDD comes up first, provided the device is held in shutdown);
4. Once power supplies are stable, start MCLK, SCLK, LRCK;
5. Configure the device via the control port in the manner required by the use case; especially bit “Format” (as “A” shown in the following figure).
6. Once power supplies and clocks are stable and the control port has been programmed, bring \SD pin High, or write bit “SD” (Bit 2 of Register 0x12) as 1;
7. The device is now in normal operation. Fade in SDIN if needed. The device is still configurable through IIC port. (as “B” shown in the following figure)

The sequence diagram is shown in Figure 15 and Table 9.

1. 通过引脚ADR[1:0]设置器件地址；
2. \SD脚拉低;
3. 接入电源（器件关断状态下，VBAT、AVDD、DVDD上电先后顺序无严格要求);
4. 当电源稳定后，开启MCLK, SCLK, LRCK;
5. 通过IIC进行正确的配置，如“Format”等（下图中的“A”）;
6. \SD脚拉高，或写bit“SD”为1 (寄存器 0x12 的Bit 2);
7. 器件进入正常工作模式。若需要可将SDIN通过渐变引入。此后仍可通过IIC进行部分配置。（下图中的“B”）

具体时序如下图 Figure 15和下表Table 9

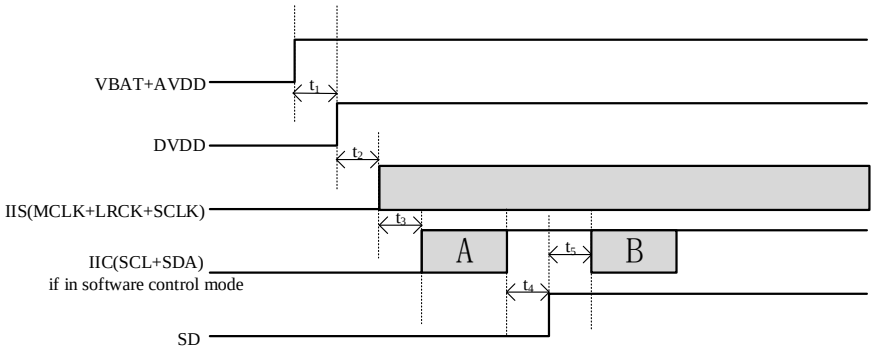



Figure 15 Power-on Sequence

Table 9 Recommendations for Power-on Timing

| Symbol | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| t1 | | 0 | | | ms |
| t2 | | 0 | | | ms |
| t3 | | 1 | | | ms |
| t4 | | 1 | | | ms |
| t5 | | 200 | | | ms |

### 6.2 Power down Procedures

1. The device is in normal operation;
2. Fade out SDIN if needed; The device is configurable through IIC port before power off;
3. Pull \SD pin Low, or write bit “SD” (Bit 2 of Register 0x12) as 0;
4. The clocks can be stopped, and power supplies brought down;
5. The device is now fully shutdown and powered off.

The sequence diagram is shown in Figure 16 and Table10.

芯片处于工作状态;

1. 若需要可将SDIN淡出;器件仍可在关闭之前通过IIC配置;
2. 将\SD脚拉低，或写bit “SD” 为0 (寄存器0x12的Bit 2);
3. MCLK, SCLK, LRCK关闭，然后电源关闭;
4. 芯片已关闭.

具体时序如下图 Figure 16和Table10.

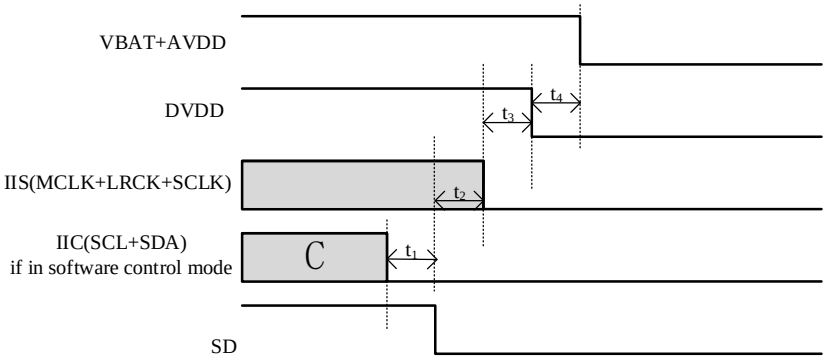
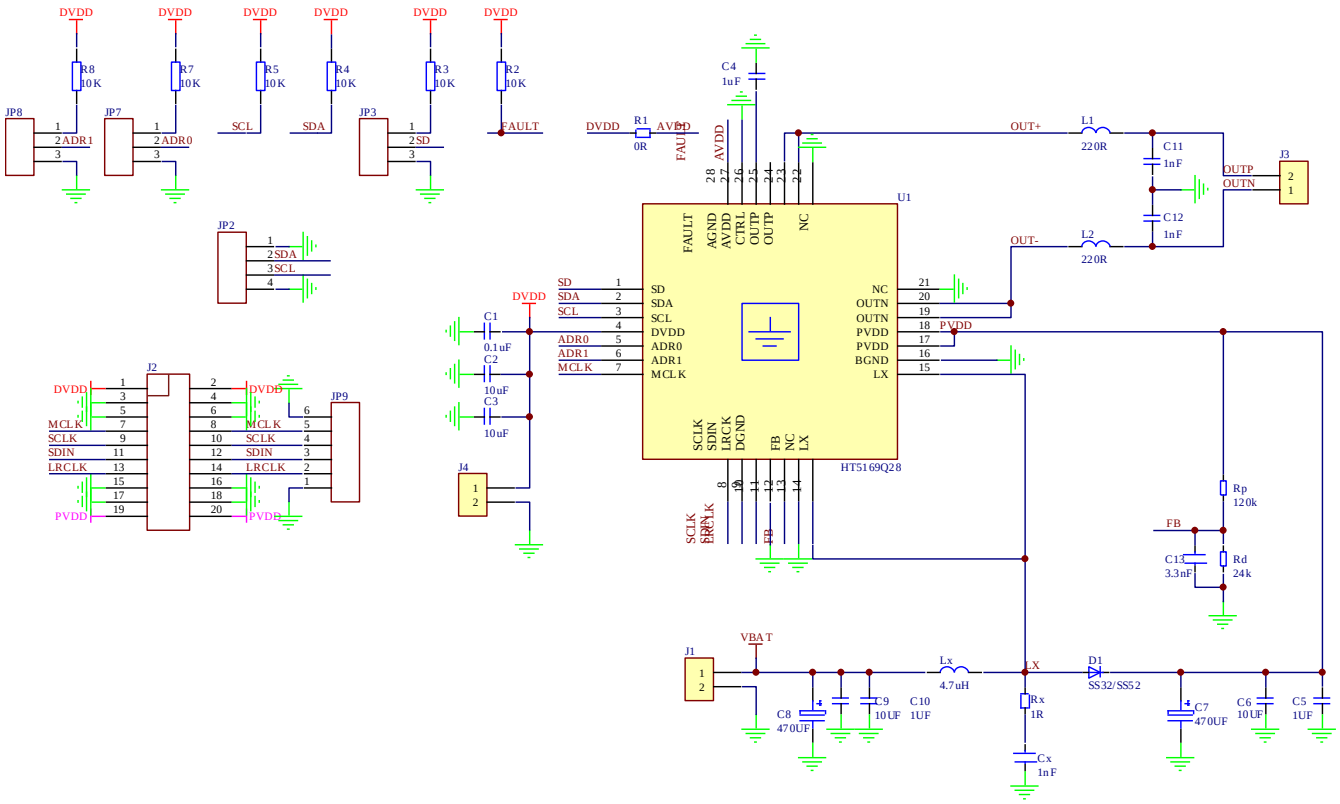



Figure 16 Power-off Sequence

Table10 Recommendations for Power-off Timing

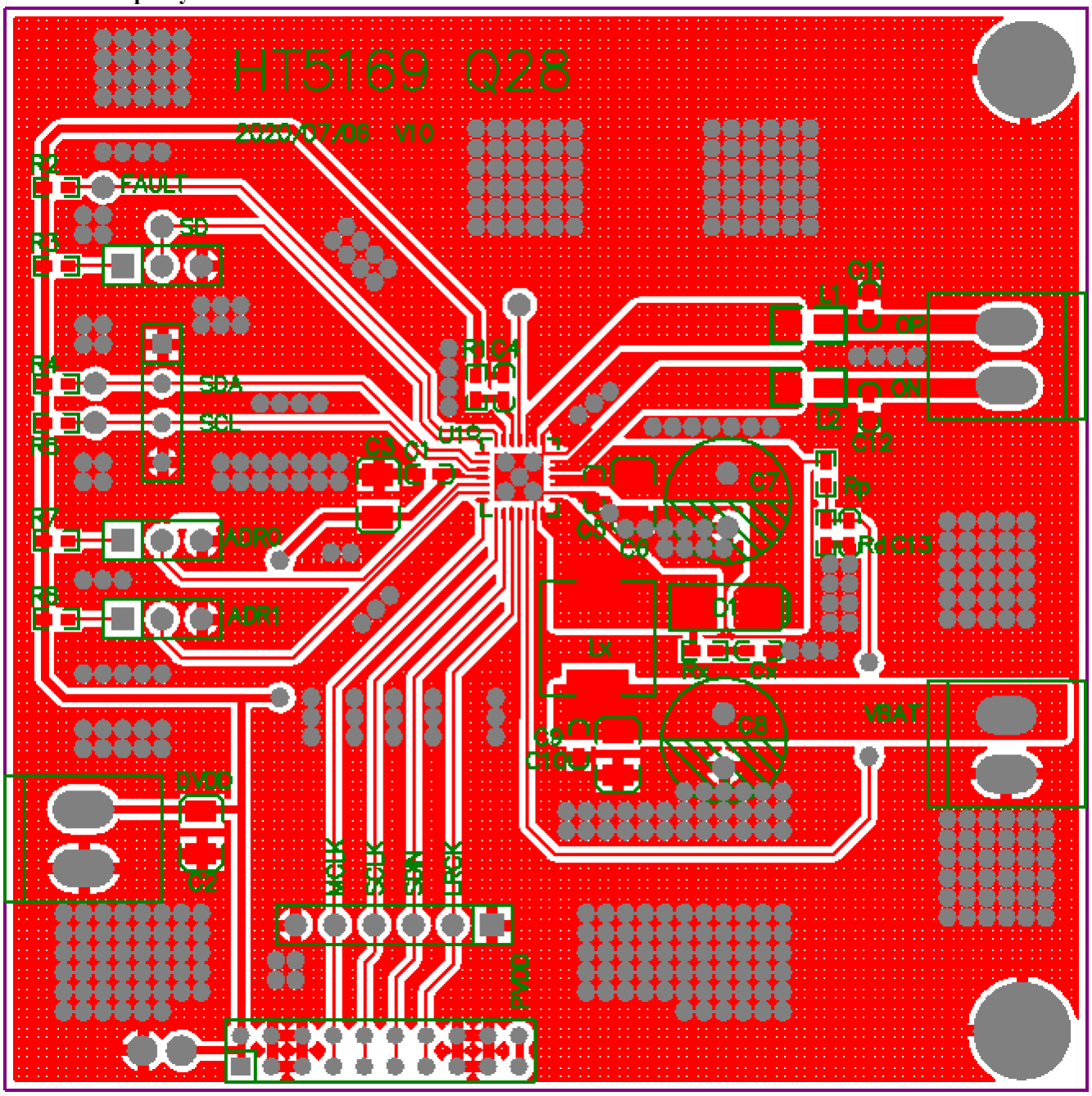
| Symbol | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_1$ | | 1 | | | ms |
| $t_2$ | Fade-out disabled | 1 | | | ms |
| | Fade-out enable | 45 | | | ms |
| $t_3$ | | 1 | | | ms |
| $t_4$ | | 0 | | | ms |

## 7 Typical Circuit Diagram

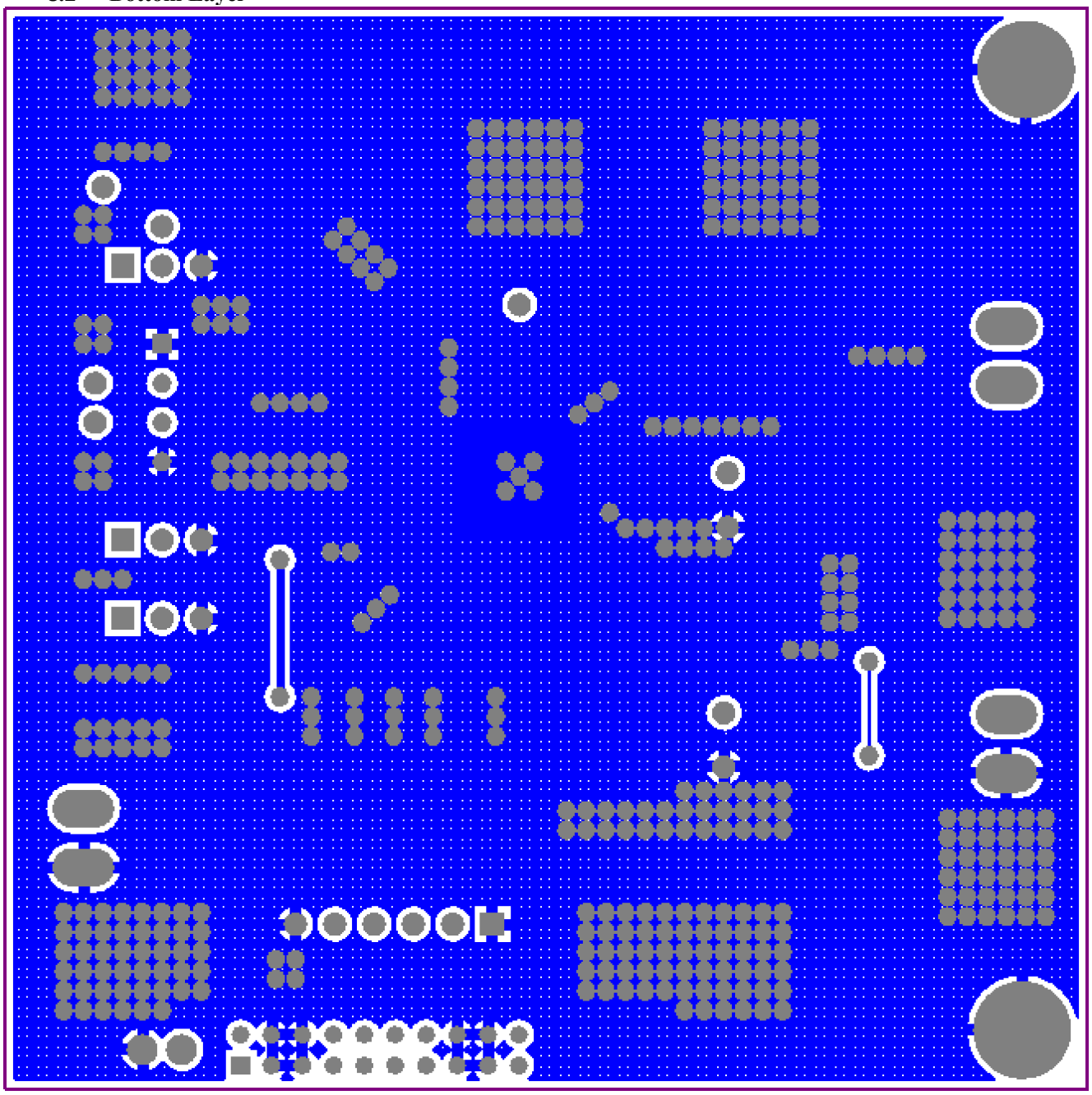


# 8 PCB Layout

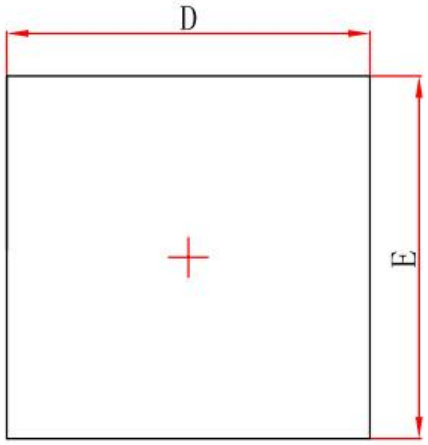
## 8.1 Top Layer



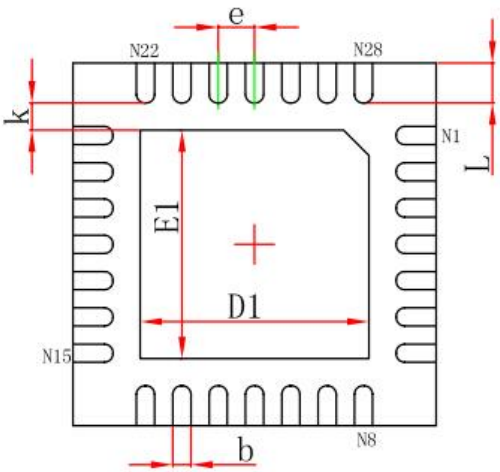
### 8.2 Bottom Layer



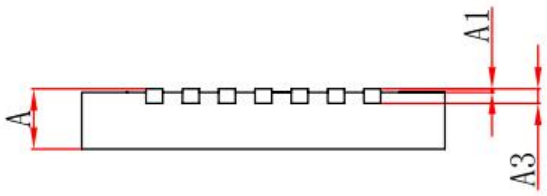
## ■ PACKAGE OUTLINE




Top View




Bottom View




Side View

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.700/0.800 | 0.800/0.900 | 0.028/0.031 | 0.031/0.035 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.203REF. | | 0.008REF. | |
| D | 4.900 | 5.100 | 0.193 | 0.201 |
| E | 4.900 | 5.100 | 0.193 | 0.201 |
| D1 | 3.050 | 3.250 | 0.120 | 0.128 |
| E1 | 3.050 | 3.250 | 0.120 | 0.128 |
| k | 0.200MIN. | | 0.008MIN. | |
| b | 0.180 | 0.300 | 0.007 | 0.012 |
| e | 0.500TYP. | | 0.020TYP. | |
| L | 0.450 | 0.650 | 0.018 | 0.026 |

## IMPORTANT NOTICE
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**嘉兴禾润电子科技有限公司**
**Jiaxing Heroic Electronic Technology Co., Ltd.**
地址: 浙江省嘉兴市凌公塘路3339号JRC大厦A座三层
Add: A 3rd floor, JRC Building, No. 3339, LingGongTang Road, Jiaxing, Zhejiang Province
Sales: 0573-82585539, sales@heroic.com.cn
Support: 0573-82586151, support@heroic.com.cn
Fax: 0573-82585078
Website: www.heroic.com.cn; wap.heroic.com.cn
Wechat MP: HEROIC_JX
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